Qualcomm Technologies International, Ltd.

QCC5229 VFBGA Hardware Design Guide

User Guide

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Revision history

Revision	Date	Change reason
AA	May 2024	Initial release.

Contents

Tables

Figures

Equations

1 Introduction

This document describes the main points to consider when designing using QCC5229 VFBGA with a particular focus on the PCB layout and component selection. An example application schematic and lists of preferred components are provided in the QCC5229 VFBGA example application schematic and BOM.

When designing a system using the QCC5229 VFBGA, the board layout can influence end-product performance. Place the following printed circuit board (PCB) components in descending order of priority:

1. The switch-mode power supply (SMPS) components
2. Bluetooth® radio frequency (RF) trace and band pass filter
3. Bluetooth RF decoupling
4. Crystal (xtal)
5. Audio reference capacitor
6. The low (voltage) drop-out (LDO) regulator decoupling
7. All other decoupling

The following symbols help navigate the necessary information for the design process:

Indicates the schematic design or component choice information. Follow the symbol in the document to find descriptions of schematic design rules and guidelines.

Indicates layout information. Follow the symbol in the document to find the necessary information for PCB routing.

2 Power management

The power management section describes the configurations and specifications of the power components of the QCC5229 VFBGA device, which includes SMPS configurations, power decoupling, charger connections (for both configurations), and powering microphones.

2.1 SMPS

The QCC5229 VFBGA has four SMPSs as described in Table 2-1.

Table 2-1 SMPS description

Supply name	Use
SMPS_ANA	System, audio, and RF
SMPS_RF	RF and audio
SMPS_MX	Digital memory
SMPS_CX	Digital core

All SMPSs have three modes of operation. The QCC5229 VFBGA automatically configures the modes depending on the integrated circuit (IC) state to minimize power consumption:

- Pulse width modulation (PWM) mode
- Pulse frequency modulation (PFM) mode
- Ultra low power (ULP) mode - a low-power PFM mode

2.1.1 Input power supply selection

The application software can configure the QCC5229 VFBGA to use either VCHG or VBAT as its internal power supply.

NOTE Select one source only for the device.

This source supplies all the internal SMPSs. Integrated low impedance reverse current safe switches to SMPS_DCPL toggle between VCHG_SMPS and VBAT_SMPS to determine the supply for the on-chip SMPSs.

Provide a low impedance path from the decoupling capacitors' (C_VCHG and C_VBAT) ground terminals back to GND. The ground path carries high frequency SMPS noise.

Layout

Place the C_DCPL1 and C_DCPL2 capacitors close to the QCC5229 VFBGA device to close the high frequency current loop and minimize electromagnetic interference (EMI). The decoupling capacitors also reduce on-chip ringing caused by unwanted PCB inductance. If SMPS_DCPL is not properly decoupled to the GND, the EMI from the SMPS is higher, and the resulting transient voltage spikes may damage the QCC5229 VFBGA.

To minimize peak currents sourced from SMPS_DCPL in pulse width modulation (PWM) mode, the PWM clock (2 MHz) waveforms are phase shifted by 90 degrees for each SMPS, see Figure 2-1.

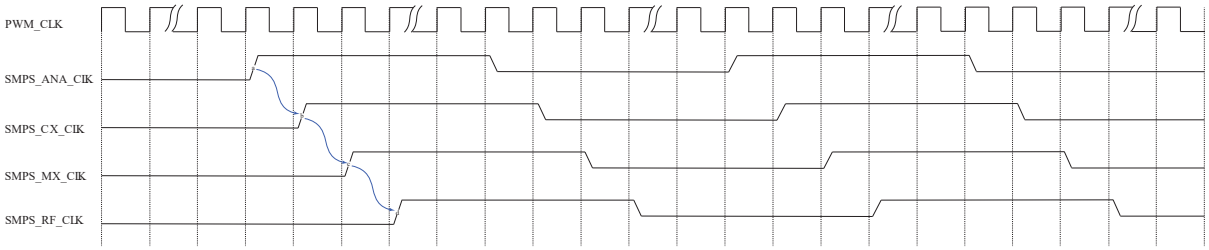

Figure 2-1 SMPS PWM clock with shifted clock phase

2.1.2 SMPS EMI emissions

The QCC5229 VFBGA has four SMPSs, each with separate current loops. Each SMPS has two main current loops during operation:

- S1 current loop: S1 is closed, see Figure 2-2

  In the S1 current loop, current flows through the V_{IN} decoupling capacitor (C1), the switch (S1), the inductor (L1), and the output capacitor (C2). As the current always flows in a loop, the return path for the current is from the ground (GND) of C2 back to the GND of C1. On the QCC5229 VFBGA, the VIN net is SMPS_DCPL.

  Equation 2-1 shows the equation for an inductor.

$$V_L = L \times \frac{dI_L}{dt}$$

Equation 2-1 Inductor equation

  For the S1 current loop, V_L equals $V_{IN} - V_{OUT}$ (ignoring losses) and L is the fixed inductor value. In this configuration, the inductor current increases linearly while switch S1 is closed.

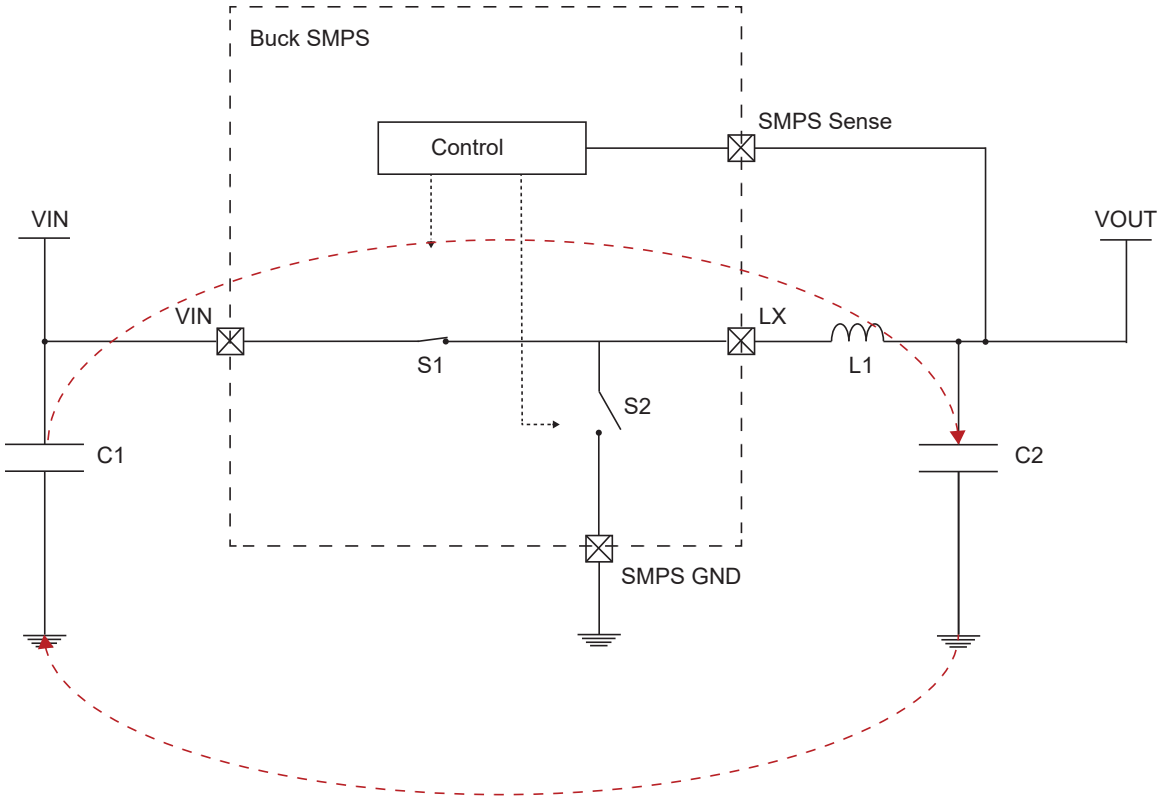

Figure 2-2 SMPS current loop - S1

- S2 current loop: S2 is closed, see Figure 2-3

  In the S2 current loop, the S1 switch is open and the S2 switch is closed. In this configuration, the inductor carries the sourcing current out of the SMPS GND node. The return path for the current in the S2 current loop is from the GND of C2 back to SMPS GND, see Figure 2-3.

For the S2 current loop, V_L is $-V_{OUT}$ (ignoring losses) and L is fixed. This configuration means that dI_L/dt is now negative and the inductor current decreases linearly.

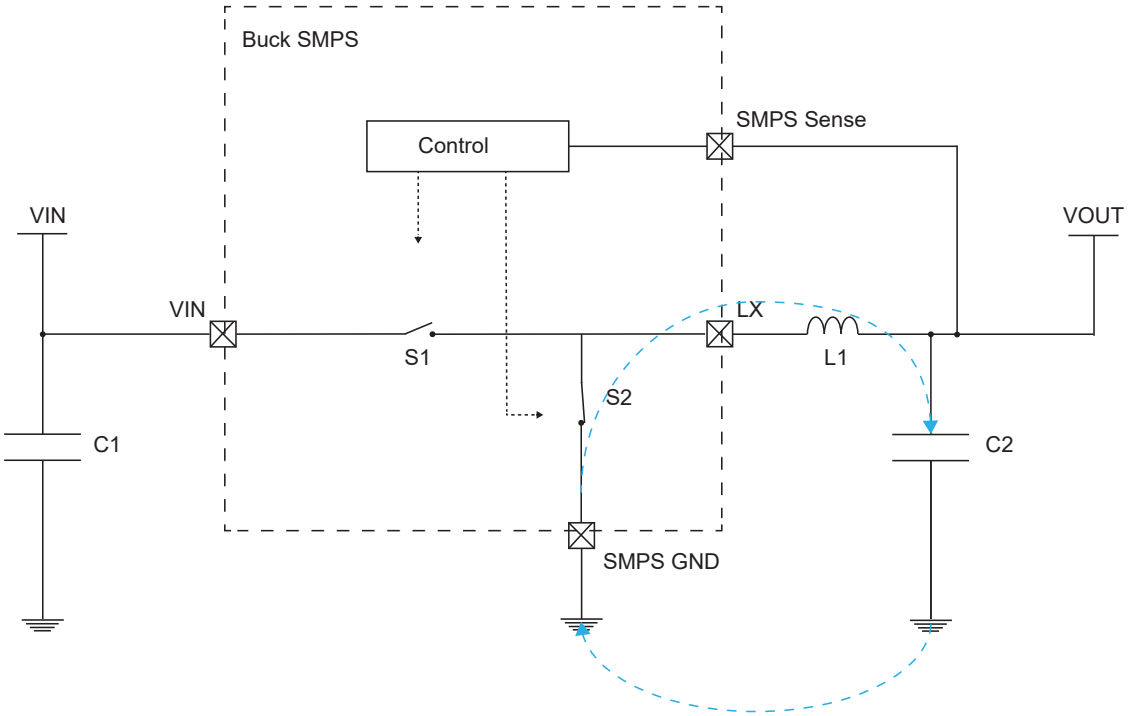

Figure 2-3 SMPS current loop - S2

The QCC5229 VFBGA SMPS senses the current flowing in switch S2. If the inductor current reaches zero, switch S2 opens to prevent the inductor current flowing in the reverse direction (from capacitor C2 to SMPS GND). This phenomenon is called discontinuous conduction mode (DCM), and increases SMPS efficiency in low load conditions.

In pulse frequency modulation (PFM) and ultra low power (ULP) modes, the SMPS frequency depends on the load current. In PWM mode, the SMPS operates with a frequency of 2 MHz. The voltage on the LX node changes between V_{IN} (SMPS_DCPL) and GND as a square wave.

S1 is turned off fast to maximize SMPS efficiency. Due to the capacitance on the LX node, the voltage changes from Vin to GND in <2 ns and therefore emits EMI radiation ranging from DC to several GHz.

Keep the SMPS current loops small to minimize EMI from the SMPS. Take the SMPS outputs from the capacitors to minimize high frequency noise on the power rail. Connect the capacitor GND firmly to the main GND plane on the PCB to ensure that the power rails are referenced to the main GND.

Avoid having any tracks below the four LX traces and the respective inductor pads. Route sensitive PCB traces away from the SMPS components and traces.

Place the decoupling capacitors close to the chip. This placement is critical to limit the voltage spikes on SMPS_DCPL caused by PCB inductance.

Minimize the area within the current loop by placing the SMPS components close to the QCC5229 VFBGA.

Figure 2-4 shows the SMPS section of the QCC5229 VFBGA reference schematic.

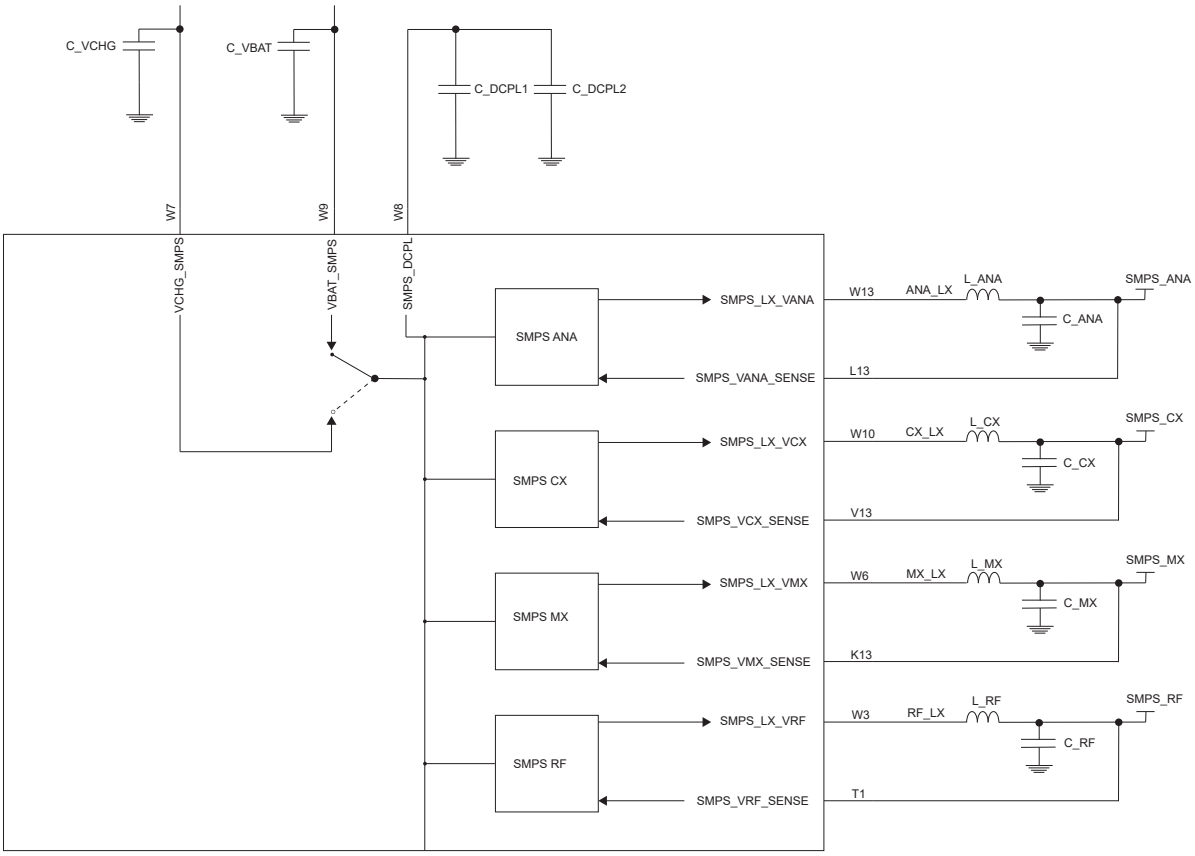

Figure 2-4 SMPS PCB schematic

Figure 2-5 shows the ideal SMPS layout for the QCC5229 VFBGA.

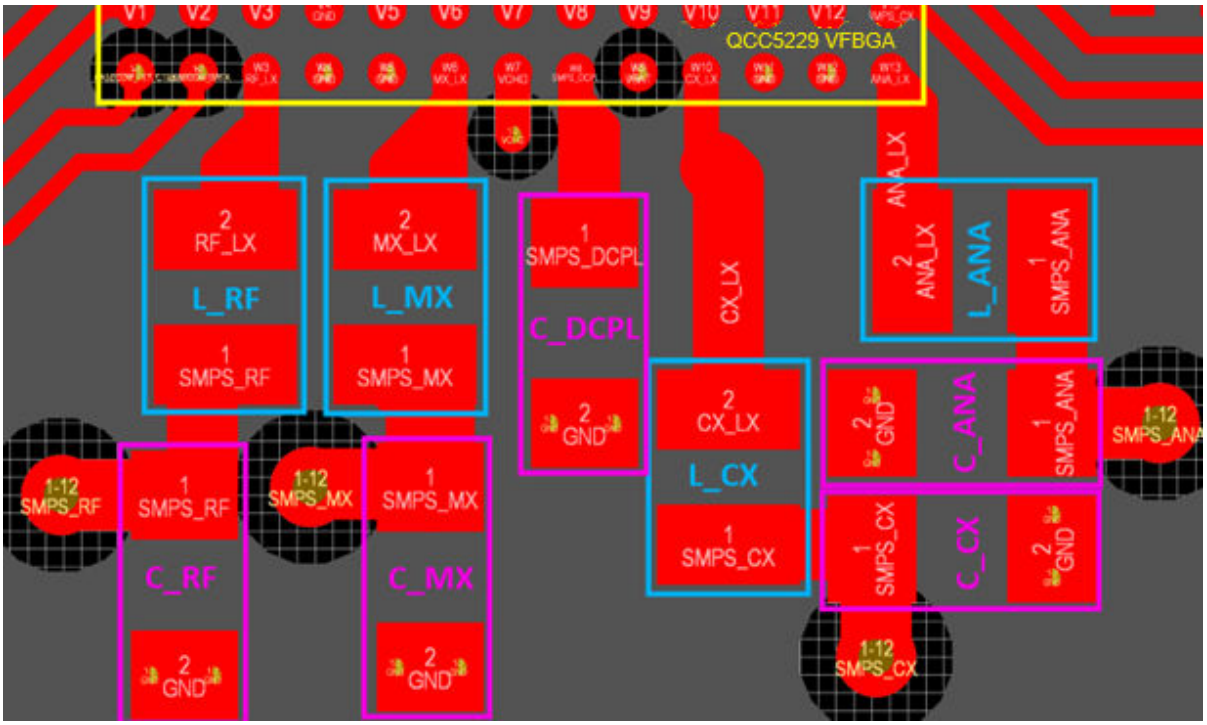

Figure 2-5 QCC5229 VFBGA SMPS layout

Figure 2-6 shows the S1 current loop created in SMPS_ANA when the S1 switch is closed.

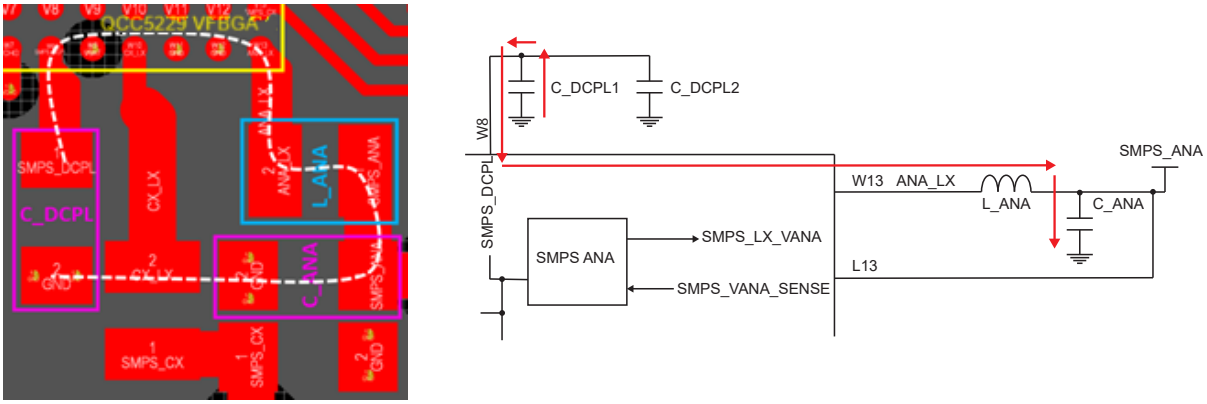

Figure 2-6 SMPS_ANA S1 current loop

Figure 2-7 shows the S2 current loop for SMPS_ANA created when the S2 switch is closed.

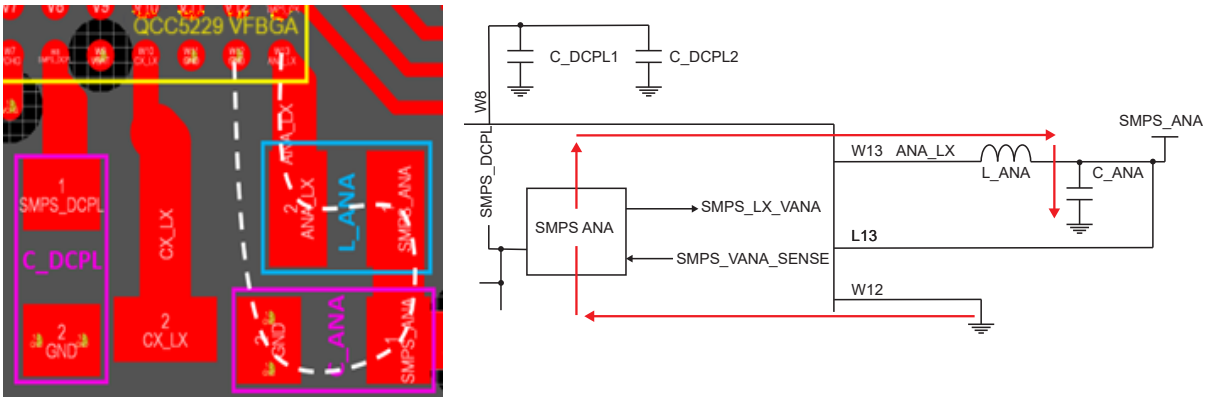

Figure 2-7 SMPS_ANA S2 current loop

Similar current loops occur for all four SMPSs.

2.2 Power supply decoupling and connections

The QCC5229 VFBGA has multiple LDOs, switchable power outputs, and decoupling nodes.

Table 2-2 lists the required capacitor and supply connections for each power pin.

The decoupling capacitor, if necessary, should be located close to the power pin.

For capacitor specification, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

Table 2-2 Required power pin connections

Use	Power pin	Decoupling capacitor	Supply
PMU	VCHG_SMPS	C_VCHG	VCHG
	VBAT_SMPS	C_VBAT	VBAT
	SMPS_DCPL	C_DCPL1, C_DCPL2	-
	LX_VANA	C_ANA	
	LX_VCX	C_CX	
	LX_VMX	C_MX	
	LX_VRF	C_RF	
	VDD_BYP	C_BYP	
	VDD_AUX_DCPL	C_AUX_DCPL	
	VDD_KA	C_KA	
	LDO_CMX	C_CMX	
	LDO_CCX	C_CCX	
	LDO_AMX	C_AMX	
	LDO_BMX	C_BMX	
	LDO_APMX	C_APMX	
	VDD_TMX	C_TMX	
	VDD_AON	C_AON	-
	LDO_LCX	C_LCX	
	LDO_HCX	C_HCX	
	VDD_MX_IN	C_MX_IN [a]	SMPS_MX
	VDD_PMU_1V8	C_PMU_1V8 [a]	SMPS_ANA
	VDD_CX_IN	C_CX_IN [a]	SMPS_CX
Bluetooth radio	VDD_BT_1V8	C_BT_1V8 [a]	SMPS_ANA
	VDD_BT_1V1	C_BT_1V1 [a]	SMPS_RF
Aux	VDD_AUX_1V8	C_AUX_1V8 [a]	SMPS_ANA
	VDD_AUX_1V1	C_AUX_1V1 [a]	SMPS_RF

Table 2-2 Required power pin connections (cont.)

Use	Power pin	Decoupling capacitor	Supply
	VDD_AUX_1V8	C_AUX [a]	SMPS_ANA
USB	LDO_USB_1V8	C_USB_1V8	-
	VDD_3V3_USB_SW	C_USB_3V3	
	USB_DVDD	C_USB_DVDD	
BRG	VDD_BRG	C_BRG [a]	SMPS_ANA
	VDD_BRG_1V8	-	
	VDD_BRG_SWR		
Flash	VDD_FLASH	C_FLASH	

[a] Optional decoupling capacitor. Required only if low inductance and low impedance connection to supply net is not possible.

2.3 Charger

The QCC5229 VFBGA has an integrated Li-ion charger that is designed to support single Li-ion cells with a wide range of cell capacities and variable V_{FLOAT} voltages.

It has two circuit configurations with different charge current capabilities:

- **Internal configuration**: Supports charge rates of up to 400 mA with no additional external components required.
- **External configuration**: Supports charge rates of 200 mA to 1.8 A with the addition of a bipolar PNP transistor and an external sense resistor. Lower trickle and precharge currents are still available in this configuration

NOTE By default, the charger configuration is internal. If necessary, enable and configure the external charger mode in the application software.

2.3.1 Charger connections

In both charger configurations, charge current enters through the VCHG pin, which should be locally decoupled with a ceramic capacitor C_VCHG. As the VCHG net is a high-voltage node, the capacitor must be appropriately voltage rated. The charger output current exits through the VBAT pin to the battery. The VBAT should be locally decoupled with a ceramic capacitor (C_VBAT). The capacitor values are specified in the *QCC5229 VFBGA Data Sheet* (80-75559-1).

C_VCHG should be placed close to the VCHG pin. C_VBAT should be placed close to the VBAT pin. The VBAT_SENSE pin is used to sense the voltage on the battery and should be routed as a star point connection (separately) to the battery connector. This star point connection avoids the IR drop in the battery PCB traces, which can lead to early termination, from affecting the charge process. Thick PCB tracks are not required as this is a sense connection.

Internal charger configuration

Schematic

In the internal charger configuration, connect the VCHG_SENSE pin to VCHG. However, if there are PCB space constraints, the VCHG_SENSE pin can be left unconnected. The CHG_EXT is left unconnected. The charge current passes through the QCC5229 VFBGA internally in all states.

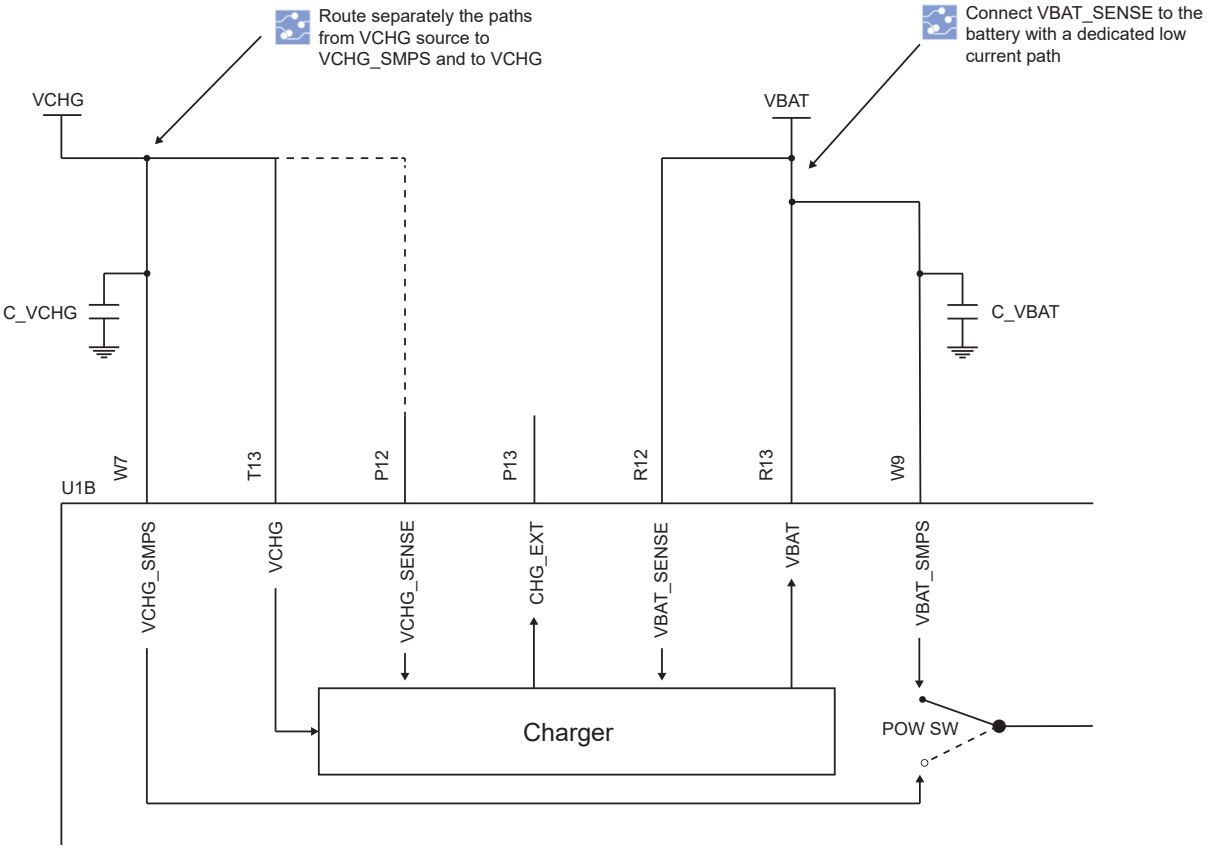

Figure 2-8 Schematic of internal charger configuration

Layout

In the internal charger configuration, the charge current can be up to 400 mA. Therefore, the VCHG and VBAT PCB tracks should be suitably sized to carry the charge current and the input power to the chip.

External charger configuration

The external charger configuration is used for enabling higher charge currents and requires an external PNP pass transistor (Q1) and a sense resistor (R_{sense}) as shown in Figure 2-9.

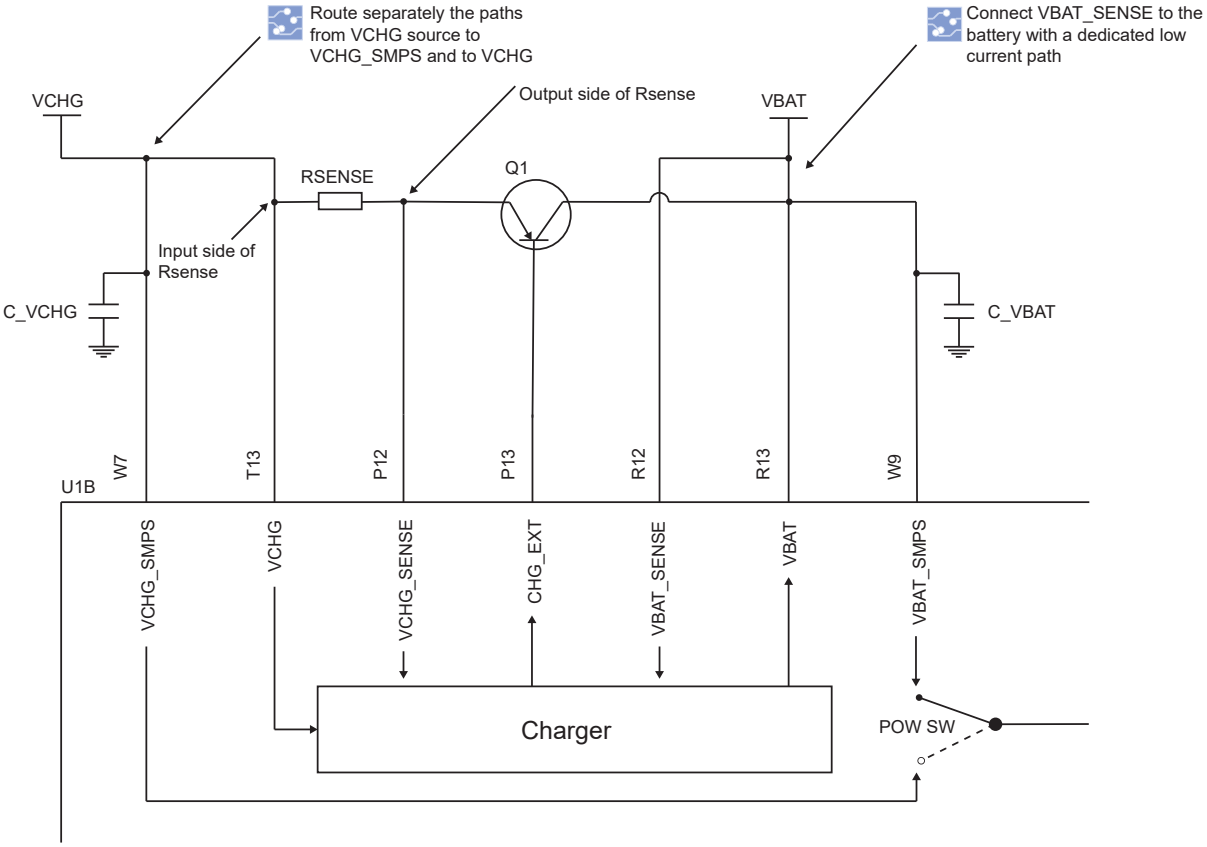

Figure 2-9 Schematic of external charger configuration

In this configuration, the QCC5229 VFBGA monitors the voltage sensed across a sense resistor R_{sense} and sinks current into the CHG_EXT to control the external transistor.

Place the R_{sense} such that its input pad is close to the VCHG pin using a low-resistance track to minimize IR drop. Connect VCHG_SENSE directly to a star point connection at the output pad of R_{sense}. Thick PCB tracks are not required as this is a sense connection.

The PCB routing around the VCHG pin and sense resistor is critical for the charge current accuracy. When the internal power switch is configured to power the VDD_BYP regulator from VCHG, the regulator current flows in through the VCHG pin. Using a star point connection to route VCHG into the device minimizes the effects of the VDD_BYP current IR drop on the charge current sense accuracy. If a star point is not used, sharing of PCB tracks leads to:

- Small increase in battery charge current dependent on the VDD_BYP current
- Inaccurate current readings
- Early termination

In the external charger configuration during the fast charge phase, the charge current can be up to 1.8 A and is routed through an external pass transistor. Therefore, the R_{sense} resistor, external transistor, and the VCHG/battery connecting PCB tracks must be suitably sized to carry the charge current. Place the external transistor close to the output pad of R_{sense}.

The QCC5229 VFBGA monitors the voltage between the VCHG and VCHG_SENSE pins. This process controls the charge current. It is important that the VCHG supply is routed to the input pin at the chip, and not routed to R_{sense} first, as this process adversely affects charge current. Excessive PCB impedance in the track appears as an additional R_{sense} resistance to the QCC5229 VFBGA and leads to lower than expected charge current.

The CHG_EXT pin can sink up to 100 mA and the tracks should be suitably sized.

Trickle and Pre-charge currents flow internally through the QCC5229 VFBGA.

Pass transistor choice

The required H_{fe} (current gain) of the pass transistor is given in the *QCC5229 VFBGA Data Sheet* (80-75559-1). High gain or Darlington devices are not suitable and may result in poor current control.

When selecting transistors, ensure that transistor H_{fe} values are quoted with 2 V V_{ce}. At low VCHG-VBAT headroom, V_{ce} can fall below this value. In this state, the QCC5229 VFBGA safely limits the maximum base current, and the charge current is reduced. This state is called REDUCED_HEADROOM.

The power dissipation in the external transistor is greatest at the transition to fast charge and maximum VCHG voltage.

Peak power dissipation in pass transistor:

$$W = \left(VCHG_{max} - V_{fast}\right) * I_{fast}$$

Equation 2-2 Peak power dissipation

A pass transistor can dissipate significant heat. Therefore, it is essential to select a device package capable of dissipating the heat generated within the device.

The PCB design should allow sufficient heatsinking of the external transistor into the board and environment, ensuring the device remains within its ratings. See, *QCC5229 VFBGA Data Sheet* (80-75559-1).

Sense resistor choice

The sense resistor determines the maximum fast charge current. Ensure accurate charge current for devices with a tolerance of 1% or lower. The resistor must be able to dissipate heat generated within it during the fast charge operation.

For maximum charge current accuracy, choose a R_{sense} resistor value, which yields a 100 mV R_{sense} voltage at the maximum appropriate fast charge current, see Equation 2-3.

After this R_{sense} value is chosen, lower fast charge currents can be selected corresponding with a R_{sense} voltage between 100 mV and 10 mV in <1 mV steps.

$$Ifast_{(ext)}(A) = 0.1\ (V)/R_{sense}\left(\Omega\right)$$

Equation 2-3 R_{sense} value

For example, a 56 mΩ resistor gives an $Ifast_{(ext)}$ maximum of ~1.78 A adjustable in ~1 mA steps down to the minimum of 200 mA.

Layout

To guarantee a particular maximum current, the PCB design should allow for 1% tolerance in the external charger circuit, and resistor tolerance of typically 1%.

For information on general charger operation, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

Unused charger

Schematic

If using an external PMIC, which provides battery charging functionality, connect the power pins as shown in Figure 2-8 for the internal charger configuration. Disconnect the VCHG_SENSE pin when the charger system is not in use.

If using a single power source to the QCC5229 VFBGA, connect this power source to either VCHG and VCHG_SMPS, or VBAT, VBAT_SMPS, and VBAT_SENSE. In this case, connecting to the VBAT net is recommended since the power switch to VBAT has a lower on-resistance as described in Input power supply selection.

2.4 Powering microphones

Microphones can be a significant contributor to system power consumption. As they are sensitive analog components, ensuring that the correct power supply is used can be critical to achieve good performance.

To minimize power consumption, it is a requirement to put microphones into a low-power state when not in use. For analog microphones, this process is done by removing their supply. Digital micro electro mechanical system (MEMS) microphones often feature a low-power suspend mode, which is activated when the clock supplied by the host is below a specified frequency. If the supply current in this low power suspend mode is still significant, then the digital MEMS microphones require the supply to be removed when they are not in use.

The power supply rejection performance of MEMS microphones varies widely, although it is higher than ECMs.

The supplies that can be selected to use with MEMS microphones are:

- SMPS ANA
- Mic bias regulator
- Digital microphone switchable power outputs
- External low dropout regulators

To minimize system power consumption, it is desirable to power microphones from SMPS ANA. If this option is selected, it is critical to ensure that the microphone has sufficient power supply rejection.

A power optimized design should attempt to leverage the power efficiency benefit of an SMPS instead of the Mic bias regulator, as this regulator draws power directly from the battery.

Use of the digital microphone switchable power outputs in the Digital microphone switchable power outputs that can yield microphone power savings compared to powering from the mic bias regulator.

2.4.1 Mic bias regulator

If ECMs are used, the mic bias regulator is recommended as the power source to meet the low-power supply noise requirements.

If the mic bias regulator is not used, the package pin should be left floating (NC).

2.4.2 Digital microphone switchable power outputs

The QCC5229 VFBGA has four dedicated switchable power outputs for use with digital microphones.

Table 2-3 Power output switches and their usage

Power output switch	Usage
VDD_1V8_DMIC_SW1	Enable the switch to supply 1.8 V only
VDD_1V8_DMIC_SW2	
VDD_1V8/1V2_DMIC_SW3	Enable the switch to supply 1.2 V in LDO mode or 1.8 V in bypass mode
VDD_1V8/1V2_DMIC_SW4	

Schematic

Decoupling capacitors are required on the switchable power outputs when used. For capacitor specification, see *QCC5229 VFBGA Data Sheet* (80-75559-1). Unused outputs can be left floating.

NOTE The voltage level of VDD_DMIC_SW3 and VDD_DMIC_SW4 are configured together. However, they can be enabled individually.

Figure 2-10 shows the digital microphone supplies.

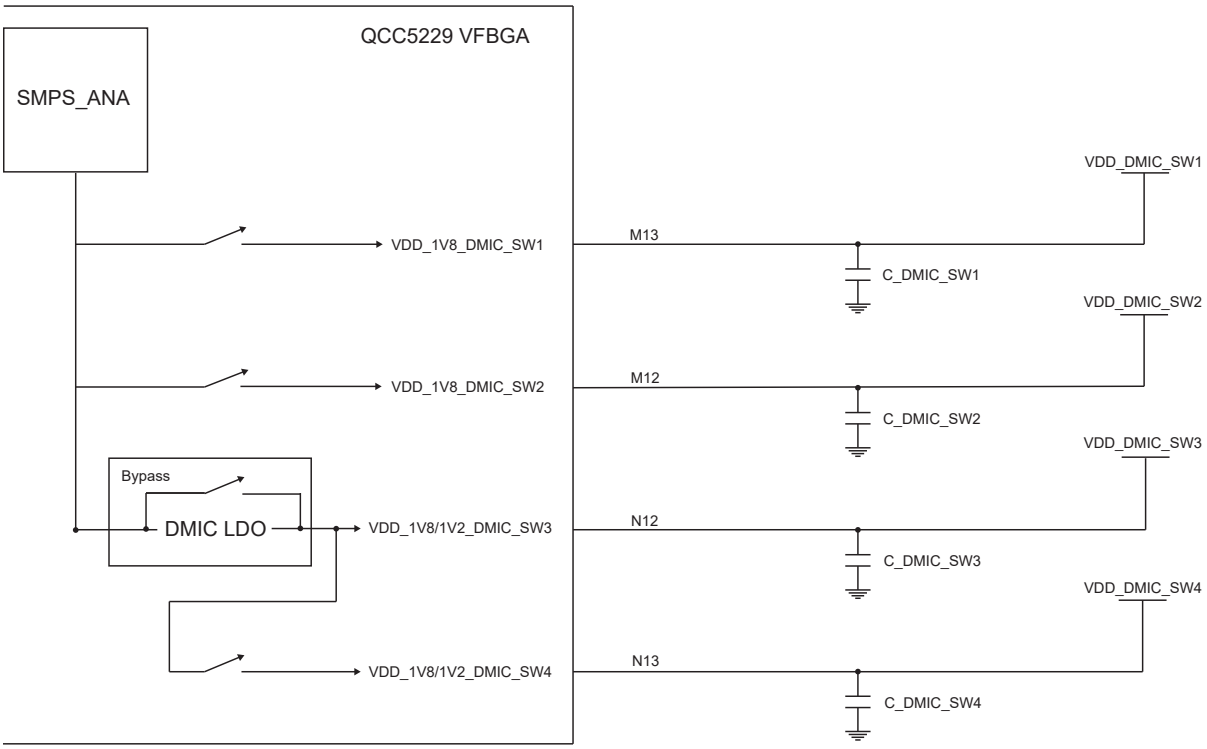

Figure 2-10 Digital microphone supplies

2.5 Powering external circuitry

The SMPS ANA rail can be used to power external circuitry in addition to internal circuitry. For maximum current output, see *QCC5229 VFBGA Data Sheet* (80-75559-1), and for the estimated device current consumption, see the ADK documentation. When powering external circuitry, configure the device to Auto or PWM mode to ensure the SMPS is not in ULP or PFM modes, which cannot support higher current limits.

When adding local decoupling capacitors to external circuitry that is powered by SMPS ANA, ensure not to exceed the maximum capacitance specified in the *QCC5229 VFBGA Data Sheet* (80-75559-1).

The QCC5229 VFBGA has an additional switchable power output, VDD_1V8_PERIPH, which can be used to power external circuitry. If VDD_1V8_PERIPH is used, place a decoupling capacitor close to the package pin. For capacitor specification, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

3 Bluetooth radio

The Bluetooth radio section describes the configurations and specifications of the Bluetooth radio components of the QCC5229 VFBGA device, which includes RF power supply unit (PSU) component, RF filter configurations, and RF layout.

3.1 RF PSU components

The QCC5229 VFBGA has an RF subsystem supplied by two rails:

- SMPS RF
- SMPS ANA

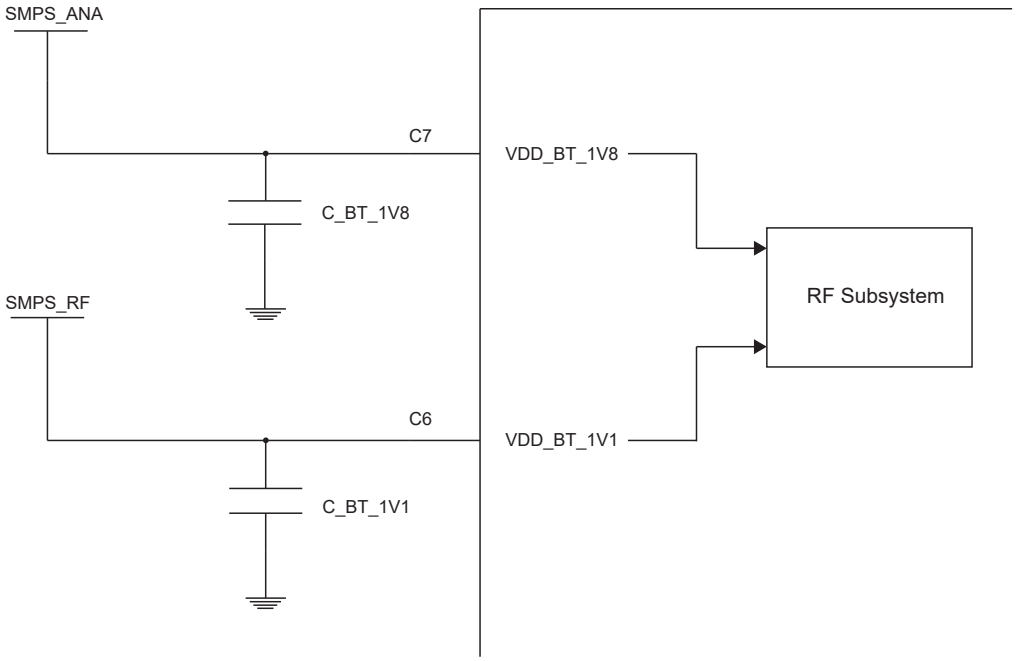

Figure 3-1 RF power supply arrangement

Schematic

If the layout allows for a low resistance and low inductance connection from SMPS ANA to VDD_BT_1V8 and SMPS RF to VDD_BT_1V1, the decoupling capacitors shown in Figure 3-1 are optional. For the VDD_BT_1V8 and VDD_BT_1V1 input capacitance specification, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

Layout

If used, place the decoupling capacitors close to their respective input pins.

3.2 RF filter

To meet the statutory emission limit, place a pi filter or a band pass filter between the RF terminal and the antenna to reduce the out of band emissions. Use an integrated filter, for example, low temperature co-fired ceramic (LTCC), surface acoustic wave (SAW) filter, or a discrete component filter. Figure 3-2 shows an example with an integrated filter.

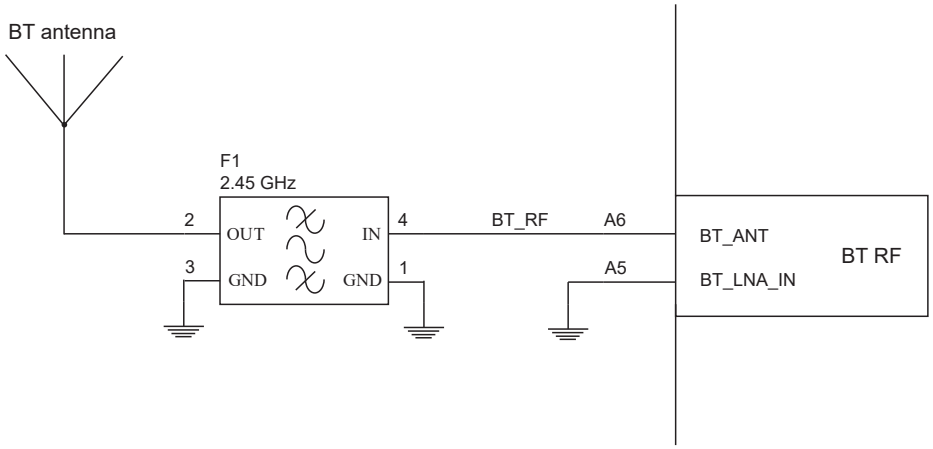

Figure 3-2 RF connection

An additional antenna matching network may be required between the filter and the antenna. For more information, see Matching network recommendations.

3.3 RF layout

The layout of the RF section in the QCC5229 VFBGA system can affect the overall RF performance. This layout holds true for ultraminiaturized designs, where radiation issues may become more important.

The ground connections become increasingly critical at RF frequencies. Connect all ground pins to the main RF reference ground plane (in metal layer L2) using microvias to minimize parasitic inductance.

Figure 3-3 shows an example RF layout reference. The routing recommendations for optimal RF performance are:

- Use the layer under the QCC5229 VFBGA chip (L2) as the main ground plane.
- Leave the pin D7 (NC) not connected.
- Connect A2 (VSS_AUX_SUBS) and pins A3 (RES) and A4 (RES) directly to the main ground plane on L2 with microvias (no connection to the ground pour on the external layer).
- Connect the pins B4 (RES) and C4 (RES) directly to the main ground plane on L2 with a microvia.
- Connect B3 (VSS_AUX) and C2 (VSS_AUX_DRIVER) to the main ground plane on L2, each with a microvia and ensure a short path between the two microvias on the layer of the main ground.
- Connect B2, C2, and B3 to the L2 GND plane.

Avoid direct connection of the RF ground across ground pins or with the ground fill on the top layer, unless expressly indicated in the instructions provided.

Figure 3-3 shows an example layout of the RF section.

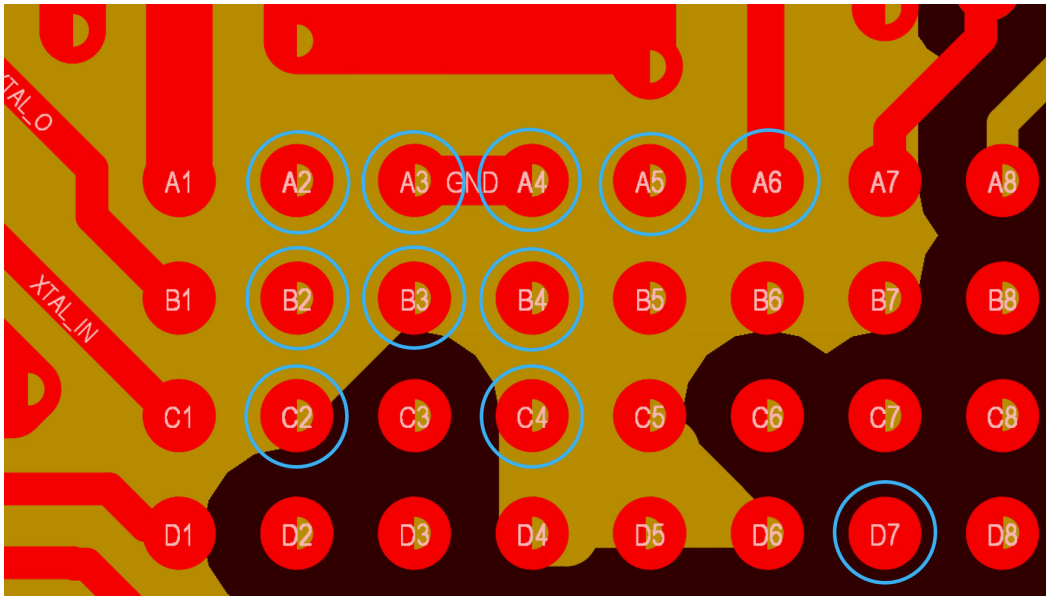

Figure 3-3 RF and xtal layout

The RF track A6 (BT_ANT) in Figure 3-3 is a coplanar waveguide designed for 50 Ω impedance and routed on the top layer. The golden colored layer is the GND plane in L2. It is important to avoid cutting or splitting the reference plane in the area below the RF track to guarantee a solid ground reference for the RF. There is no requirement to isolate this area; the L2 ground plane should extend over the whole board with the minimum amount of disruption.

3.4 Matching network recommendations

The use of a high Q T-network or LCLC matching network is recommended as both these networks can be suitably designed to achieve low insertion losses and minimal BOM cost.

If a pi-matching network is used, the EMI compliance is much more dependent on the ground return path of the first shunt capacitor and requires careful layout considerations. Figure 3-5 shows the example ground return path.

To reduce the effect of layout dependency, a provisional footprint to add a series inductor is recommended in addition to the conventional pi-matching network.

Figure 3-4 shows the suggested network from the RF output pin of the QCC5229 VFBGA.

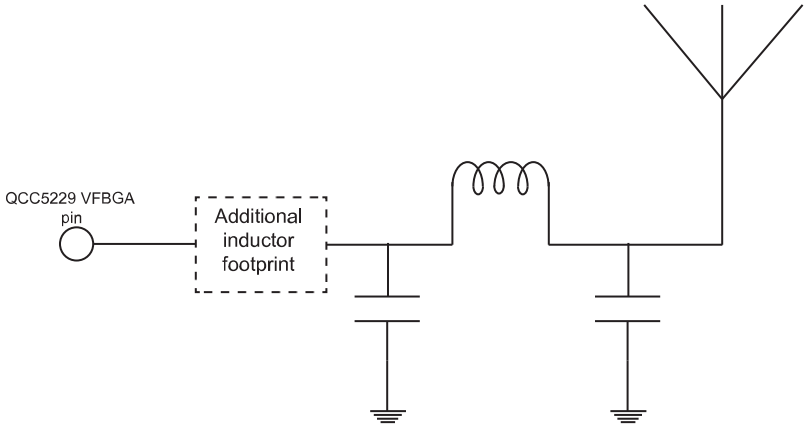

Figure 3-4 QCC5229 VFBGA LCLC matching network

T-networks exhibit less dependency on the PCB layout but to the detriment of insertion losses. A notch filter can be incorporated to expand the T-network, helping to ensure EMI compliance can be achieved with a degree of flexibility but at the expense of BOM cost and increased insertion losses. Insertion losses can be mitigated by moving to an LCLC network.

The recommended PCB layout guidance for the first shunt capacitor in any network, shown in Figure 3-5, should be to route the RF ground close to the input RF track to minimize EMI. Any turns in the RF ground trace should not exceed 45° angles.

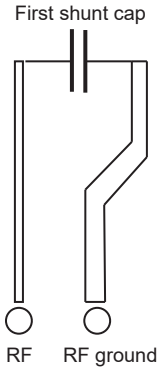

Figure 3-5 Recommended RF ground return routing

4 Crystal layout

The QCC5229 VFBGA uses a 38.4 MHz external crystal. For more information on the crystal parameter specification, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

For crystal layout, keep the tracks from XTAL_OUT and XTAL_IN short. Maintain a good ground reference on the layer below. If possible, provide a ground shield around the crystal and tracks as shown in Figure 4-1. The shortest path to GND should never be through the crystal pins.

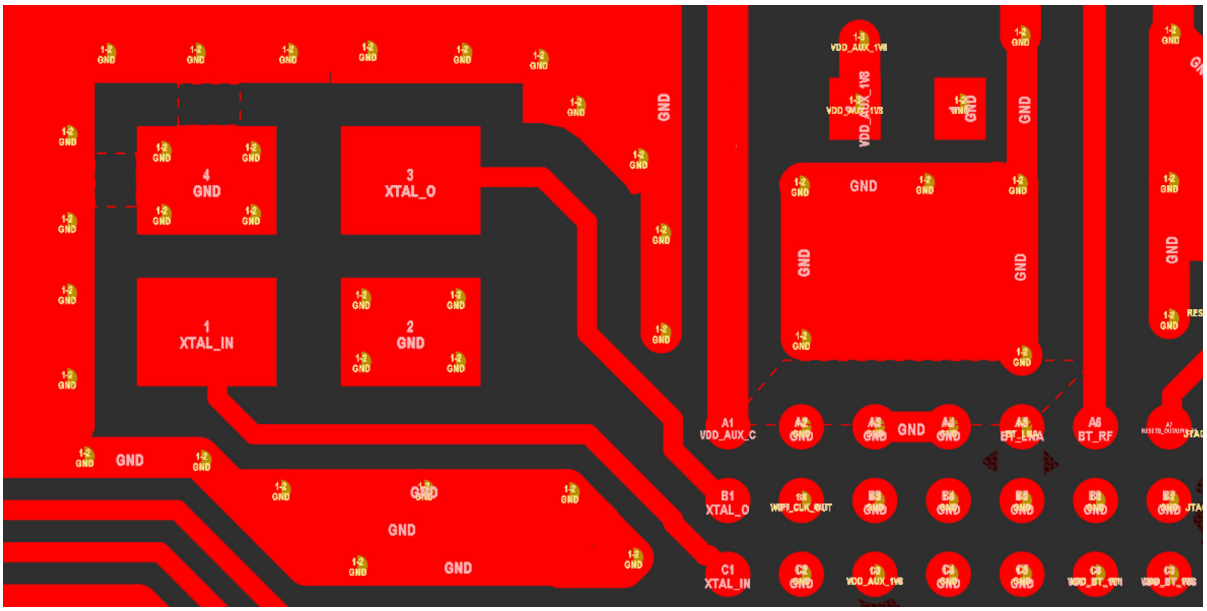

Figure 4-1 Crystal layout

5 Audio

The QCC5229 VFBGA has integrated analog audio, with three ADCs and two DACs. The DAC features a bridge-tied load (BTL) Class-D/AB output stage for directly driving a headset/speaker. To achieve optimal audio performance, ensure correct audio component placement and PCB routing.

5.1 Line inputs and outputs

The QCC5229 VFBGA has three ADCs, which can be used in differential or single-ended mode. Ground the negative input line-in (AUDIO_IN_N) in single-ended mode. Connect both inputs (AUDIO_IN_N/P) to the ground if the line-ins are not used.

NOTE The QCC5229 VFBGA ADCs does not require DC blocking capacitors when connecting to QCC5229 VFBGA ADC inputs. Microphone outputs can be connected directly to the ADC input pins without any external components.

The QCC5229 VFBGA line-outs are stereo differential outputs. In Class-D mode, the outputs can drive up to 11 mW and 22 mW into 32 Ω and 16 Ω loads respectively. In Class-AB mode, the outputs can drive 30 mW into both 32 Ω and 16 Ω loads.

A Class-AB output can be used to drive high impedance loads such as line-out applications that use an external amplifier. For applications requiring external power amplifiers, filter the Class-AB output using a 30 kHz RC low pass filter.

For designs requiring dual DAC support to drive multiple speakers, in single driver operation use-cases, the left channel DAC should be used. See the following assignments:

- AUDIO_DAC_LN/LP: assigned to Woofer
- AUDIO_DAC_RN/RP: assigned to Tweeter

There are different audio pin connection requirements depending on the DAC/ADC functionality and configuration used. Table 5-1 lists the required connections when either the DAC or ADC is used. These do not have dependency on the DAC mode.

Table 5-1 DAC/ADC mode connection requirements

Audio pin	DAC or ADC used	Neither used
VDD_AUDIO_1V8	SMPS ANA, C_AUD_1V8	SMPS ANA
VDD_AUDIO_1V1	SMPS RF, C_AUD_1V1	SMPS RF

Table 5-2 lists the required connections for the different DAC modes. These requirements are valid independent of ADC usage. The ADC relies only on the connections shown in Table 5-1. For capacitor values, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

Table 5-2 DAC mode connection requirements

Audio pin	Class-D	Class-AB	Not used
VDD_AUDIO_RX_1V8	SMPS ANA, C_AUD_RX [a]		SMPS ANA
VDD_AUDIO_HPL_1V8	SMPS ANA, C_HPL_1V8 [a]		
VDD_AUDIO_HPR_1V8	SMPS ANA, C_HPR_1V8 [a]		
VDD_AUDIO_HP_LDO_IN	SMPS RF, C_HP_1V1 [a]		SMPS RF
VDD_AUDIO_HP_LDO_OUT	C_HP_LDO	SMPS RF	SMPS RF
VDD_AUDIO_HPL_1V1/1V8	VDD_AUDIO_HP_LDO_OUT, C_HPL_1V1 [a]	SMPS ANA, C_HPL_1V1 [a]	
VDD_AUDIO_HPR_1V1/1V8	VDD_AUDIO_HP_LDO_OUT, C_HPR_1V1 [a]	SMPS ANA, C_HPR_1V1 [a]	
AUDIO_REF	C_AREF		NC

[a] Capacitor is only required if a low impedance path cannot be provided from the supply.

Layout

Place the decoupling capacitors close to the package pin to minimize voltage disturbances.

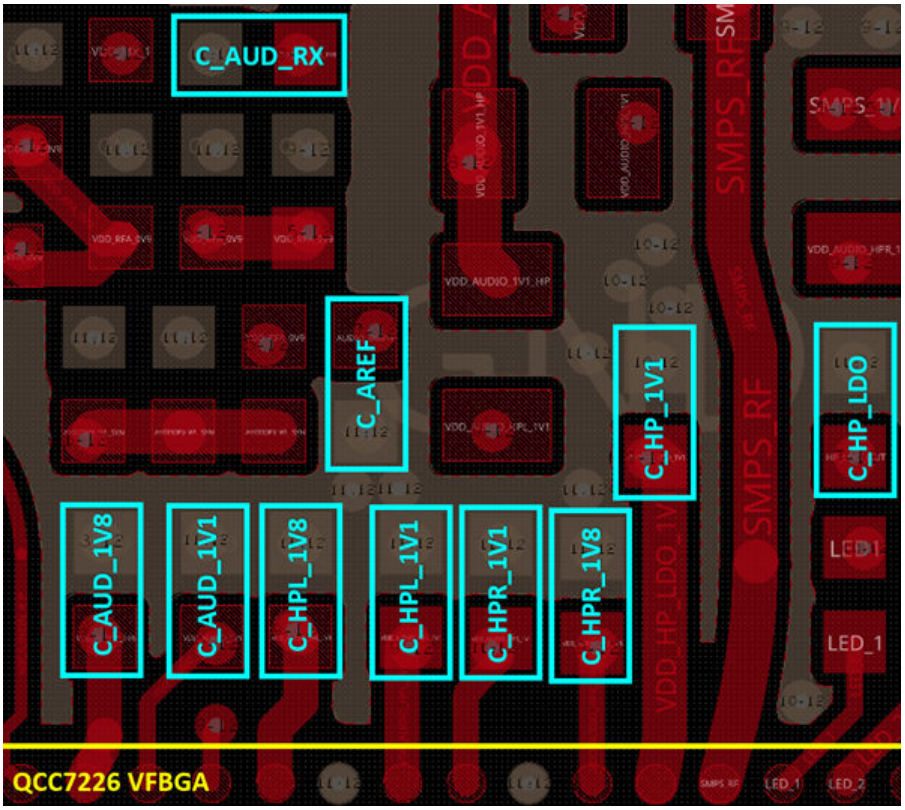

Figure 5-1 Example audio layout

Layout

The audio bandgap bypass capacitor (C_AREF in Figure 5-1) directly connects to the output of the audio voltage reference and the current generator. This connection removes flicker noise (also called 1/f noise). Any noise on the audio references couples directly into the audio. The tracks and grounding of C_AREF are critical. Place the C_AREF close to the AUDIO_REF pin to minimize the track length and ensure a short return path to VSS_AUDIO_REF. Route it far away from noisy traces to minimize noise pickup.

Layout

The Class-D amplifier is a switching circuit, ensure to route the tracks and return grounds from the QCC5229 VFBGA to the decoupling capacitors before connecting to the supply rails. The recommended layout for the line-outs and line-ins is differential routing, keeping all channels isolated from each other and from other sensitive circuitry. They should be routed to minimize track impedance and therefore IR drops, which decrease the expected power level. Locate the decoupling capacitors close to the package pin to minimize voltage disturbances.

In Class D mode, the DAC signals are sensitive and should be routed away from other noisy traces.

For more information on line/mic input, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

5.2 Digital microphone interfaces

Figure 5-2 shows the five digital microphone interface connections.

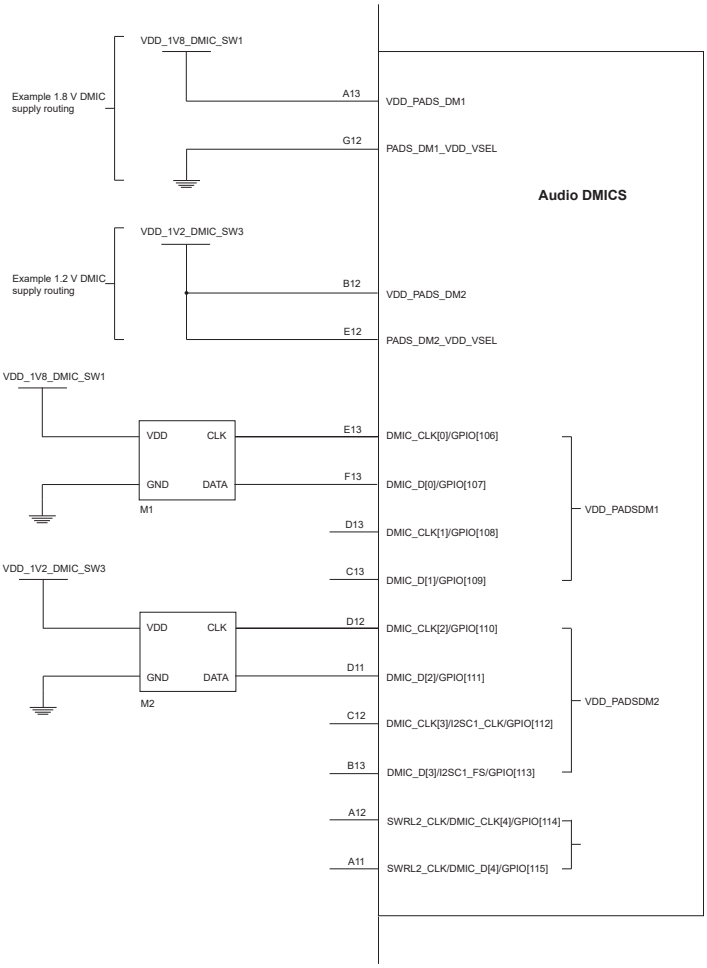

Figure 5-2 Digital microphone connections

The DMIC[0] and DMIC[1] interfaces are part of the VDD_PADS_DM1 domain. The DMIC[2] and DMIC[3] interfaces are part of the VDD_PADS_DM2 domain. Supply the VDD_PADS_DMx at the same logic level as the digital microphone interface.

The required connection for PADS_DM_VDD_VSEL depends on the voltage setting of the corresponding VDD_PADS_DM pin. It should be grounded for 1.8 V logic or connected to 1.2 V for 1.2 V logic.

The DMIC4 interface is 1.8 V only and does not require voltage level selection.

Connect VDD_PADS_DM1 and VDD_PADS_DM2 to the same rail used to supply the digital microphone domain that it is connected to, see Figure 5-2.

Decoupling capacitors for VDD_PADS_DMx are only required if a low impedance path cannot be provided from the supply rail to the package pin.

All DMIC interfaces can be left unconnected (NC) if they are not required. Ground VDD_PADS_DMx and PADS_DMx_VDD_VSEL if they are not used.

The DMIC clock signals are sensitive and should be routed away from other noisy traces.

6 GPIO

The GPIO section describes the PADS interfaces of the QCC5229 VFBGA device.

6.1 PADS interfaces

Decoupling capacitors are only required on the VDD_PADS pin if a low impedance connection to the supply rail is not possible, or if a high-speed interface is used. The required capacitance depends on which interface is used. Ensure that the decoupling capacitance is sufficient to maintain the local supply voltage.

Unused GPIOs can be left floating. For a list of default GPIO pull up/down states, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

When none of the GPIO corresponding to their VDD_PADSx domain are used, connect the VDD_PADSx pin to SMPS_ANA.

7 Reset pin (RESETB)

The QCC5229 VFBGA provides an active low chip reset function on the RESETB pin. On-chip glitch filtering avoids unintended resets by filtering out spurious noise.

The RESETB pin can be left unconnected if unused.

For more information on the RESETB pin, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

8 SYS_CTRL

The SYS_CTRL is tolerant of VBAT voltages and can connect through a button to VBAT.

When connected to VBAT using a button or driven from another IC, a series resistor R_SYS_CTRL (see Table 8-1) is required. This series resistor reduces the rise time of the signal to prevent triggering an ESD clamp on the SYS_CTRL pin as shown in Figure 8-1.

The SYS_CTRL has no internal pull-down resistor and requires an external pull-down, R_PD when connected to a button or left undriven, see Table 8-1.

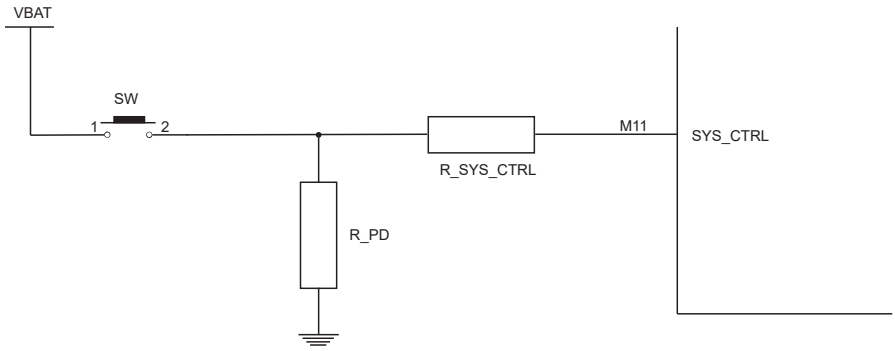

Figure 8-1 SYS_CTRL connected to resistor in series

Table 8-1 External pull-down values of sys_ctrl

Parameter	Min	Typ	Max	Unit
Resistance R_SYS_CTRL	50	100	-	kΩ
Resistance R_PD	0.01	2	-	MΩ

For more information on SYS_CTRL, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

9 LED pads

The QCC5229 VFBGA has four LED pads. These pads are configurable into four different operating modes:

- LED driver
- Digital/button input
- Analog input
- Disabled

9.1 LED driver

Schematic

This mode is designed for driving LEDs. The pad is VCHG tolerant and operates as an open-drain pad. Connect the LED cathode to the QCC5229 VFBGA LED pad as shown in Figure 9-1.

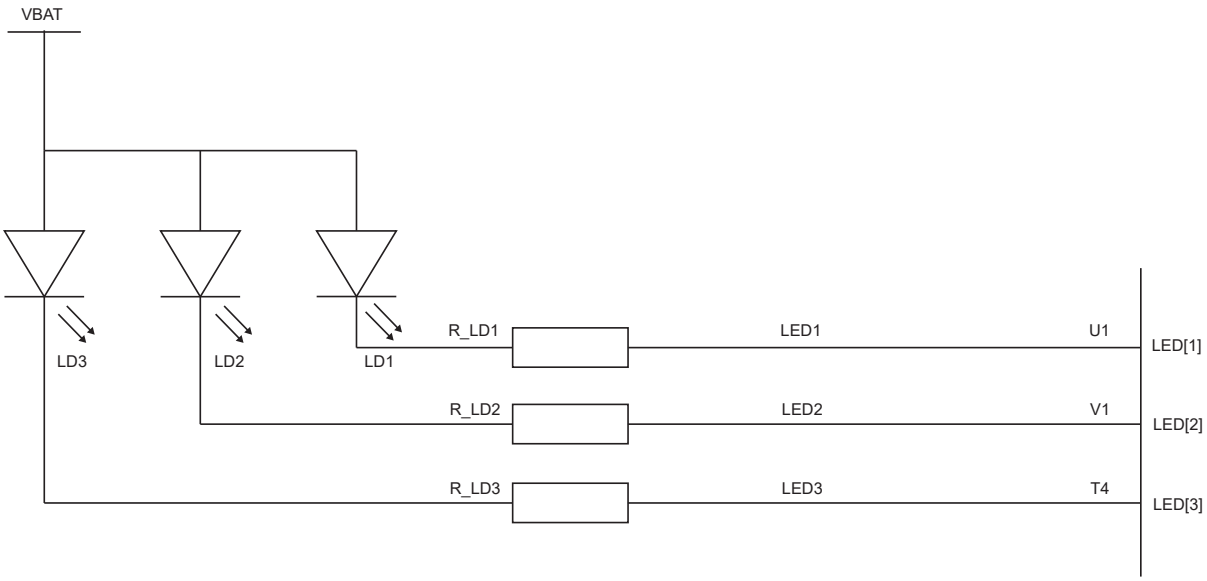

Figure 9-1 LED connections

Layout

Each pad is rated to sink up to 50 mA of current. The PCB routing should ensure that the tracking has sufficient current capacity.

NOTE As there is high current capability, these pads can perform fast edge switching. The effects of noise from PWM operation of the LEDs should be considered.

9.2 Digital/button input

The digital/button input mode is designed for slow input signals, such as buttons. It is not designed for fast-switching digital inputs such as SPI. Use the GPIOs for fast switching digital inputs.

In this mode, enable an internal weak pull-down. This setting can be used for active high button signals to ensure the input returns to 0 when the button is released.

In this mode, the pads are VCHG tolerant.

9.3 Analog input

In analog input mode, the LED pad is used as an analog input port. The pad voltage is routed to the 10-bit auxiliary ADC.

NOTE In analog input mode, the input range is 0 V to 1.8 V. If input voltages exceed 1.8 V, it may cause damage.

9.4 Battery thermistor

An NTC thermistor can be used with the LED[0] pin to directly sense battery cell temperature.

When selecting an NTC thermistor, the range of resistance should be chosen to ensure accurate measurement over the appropriate range of temperatures. The minimum resistance of the NTC thermistor should be 1k Ω at the highest temperature and the maximum resistance should be 120k Ω at the lowest temperature.

Table 9-1 lists the measurement accuracy over the supported resistance ranges.

Table 9-1 Measurement accuracy vs. temperature range

Resistance range (Ω)	Measurement accuracy
$10k \leq R_{th} \leq 120k$	± 5 %
$1k \leq R_{th} \leq 10k$	± 30 %

NOTE The measurement accuracy has more dependence on the Beta tolerance than the resistance. Choose a part with less than 5% Beta tolerance (recommended).

Table 9-2 contains a list of recommended NTC thermistors.

Table 9-2 Recommended NTC thermistors

Manufacturer part number	Resistance at 25°C (Ω)	Resistance tolerance (%)	β value (K)	β tolerance (%)
NTCS0402E3103FLT	10k	± 1	3490	± 3
NT04104F3435B1H	10k	± 1	3435	± 3
NT04104F3435B1F	10k	± 1	3435	± 1

Table 9-3 shows the measurement accuracy with respect to temperature for the example part NTCS0402E3103FLT.

Table 9-3 NTCS0402E3103FLT measurement accuracy vs. temperature range

Temperature range	Measurement accuracy
-10°C to 40°C	± 3°C
-10°C to 60°C	± 5°C

The battery thermistor can be directly connected to the LED[0] pin, which can be configured as a constant current source to provide 10 µA to the thermistor and measure the voltage across it. Figure 9-2 shows an example thermistor schematic connection.

NOTE Only LED[0] can be used for direct voltage sensing of an NTC thermistor.

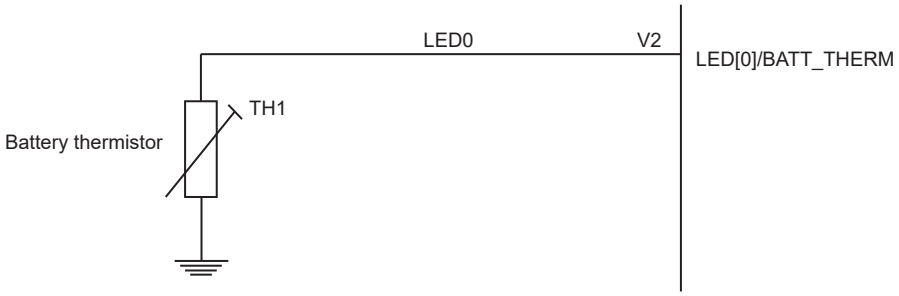

Figure 9-2 Example QCC5229 VFBGA NTC thermistor schematic connection

9.5 Disabled

By default, the state of the LED pads is disabled. The pad is VCHG tolerant and high impedance, with no pull-down.

Ground the LED pads if not used.

10 Case communications

QCC5229 VFBGA supports fast case-earbud communication (Scheme B) using only the VCHG and GND connections to pass information between a charger case and earbuds. For more information on the case communications protocol, and associated hardware and software, see *QualcommCharger Case Communication Specification* (80-21985-1).

Layout

The CASECOM_DATA is rated to sink up to 50 mA of current. The PCB routing should ensure that the tracking has sufficient current capacity.

10.1 Case communications P-MOSFET selection

When selecting a P-channel enhancement mode MOSFET device for case communications, the impact on the charger headroom condition and efficiency should be considered.

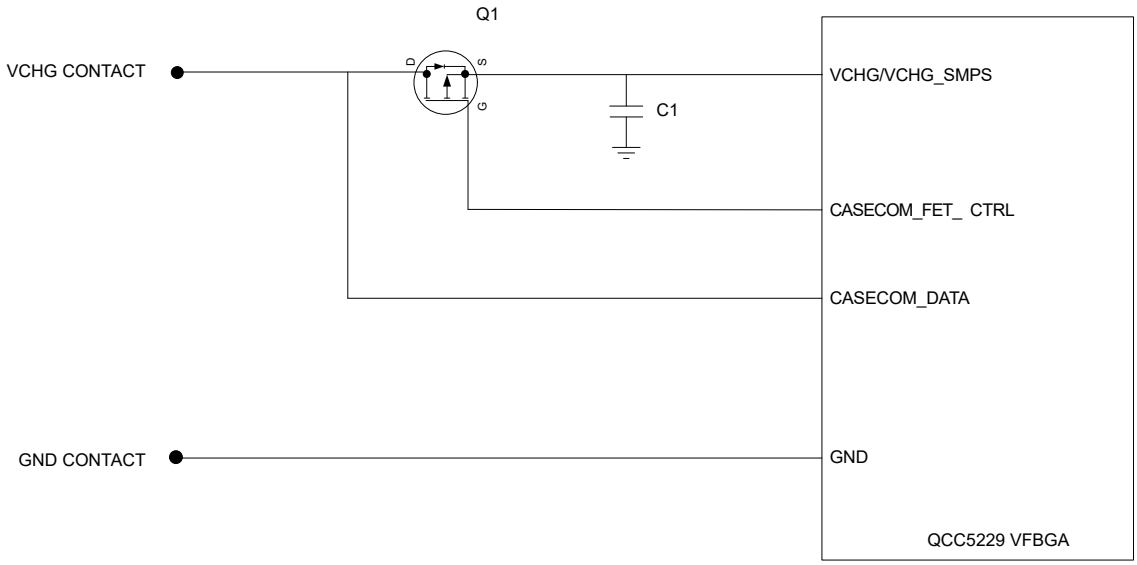

Figure 10-1 QCC5229 VFBGA case communications circuit diagram

10.1.1 MOSFET impact on charger headroom

The MOSFET should be selected with an R_{DS_on} in accordance with Equation 10-1 so it does not reduce the voltage at the charger input beyond the minimum charger headroom specification:

$$R_{DS\_on\_max} = \frac{V_D - (V_{FLOAT} + V_{HEADROOM})}{I_{LOAD} + I_{FAST}}$$

Equation 10-1 MOSFET selection

Where:

- V_D is the drain voltage of the MOSFET
- V_{FLOAT} is the configurable charging float voltage
- $V_{HEADROOM}$ is the minimum headroom voltage required by the charger
- I_{LOAD} is the peak system load
- I_{FAST} is the maximum charging current, referred to as fast charge current

The QCC5229 VFBGA peak system load (I_{LOAD}) should be determined from the respective ADK release depending on the use case.

For more information on the minimum headroom specification, see *Charger subsystem* in *QCC5229 VFBGA VFBGA Data sheet* (80-75559-1).

For example, the maximum MOSFET R_{DS_on} value is 1.38 Ω if:

- 2C fast charging is used with a 45 mAh battery
- V_{FLOAT} of 4.2 V
- V_D of 4.75 V
- Peak load of 200 mA
- $V_{HEADROOM}$ of 150 mV to charge up to 100 mA internal fast charge

10.1.2 MOSFET impact on charger efficiency

The other impact of the MOSFET is on the charging efficiency. The charger efficiency can be calculated as the charging power divided by the total power dissipated. The total power dissipated is a function of the R_{DS_on} of the MOSFET and therefore can be minimized by selecting a device with low on-resistance.

The charging efficiency is also recoverable by reducing the charger dissipation, which can be achieved by operating at the minimum headroom condition to decrease the voltage difference between the VCHG and VBAT pins of the charger.

11 USB interfaces

The QCC5229 VFBGA has one USB device interface (an upstream port, for connection to a host phone/PC or battery charging adapter).

11.1 USB device port

The device port is a USB 2.0 high speed (480 Mbps) port. In use cases such as audio source / sink / HID, the QCC5229 VFBGA enumerates as a compound device operating as a hub. The enabled audio source / sink / HID / mass storage device appears behind this hub.

The DP 1.5 k pull-up is integrated in the QCC5229 VFBGA. Series resistors are not required on the USB data lines.

Schematic

The CC pins of the USB connector can be connected to any of the AIO pins to detect the current available from the USB source, as shown in Figure 11-1.

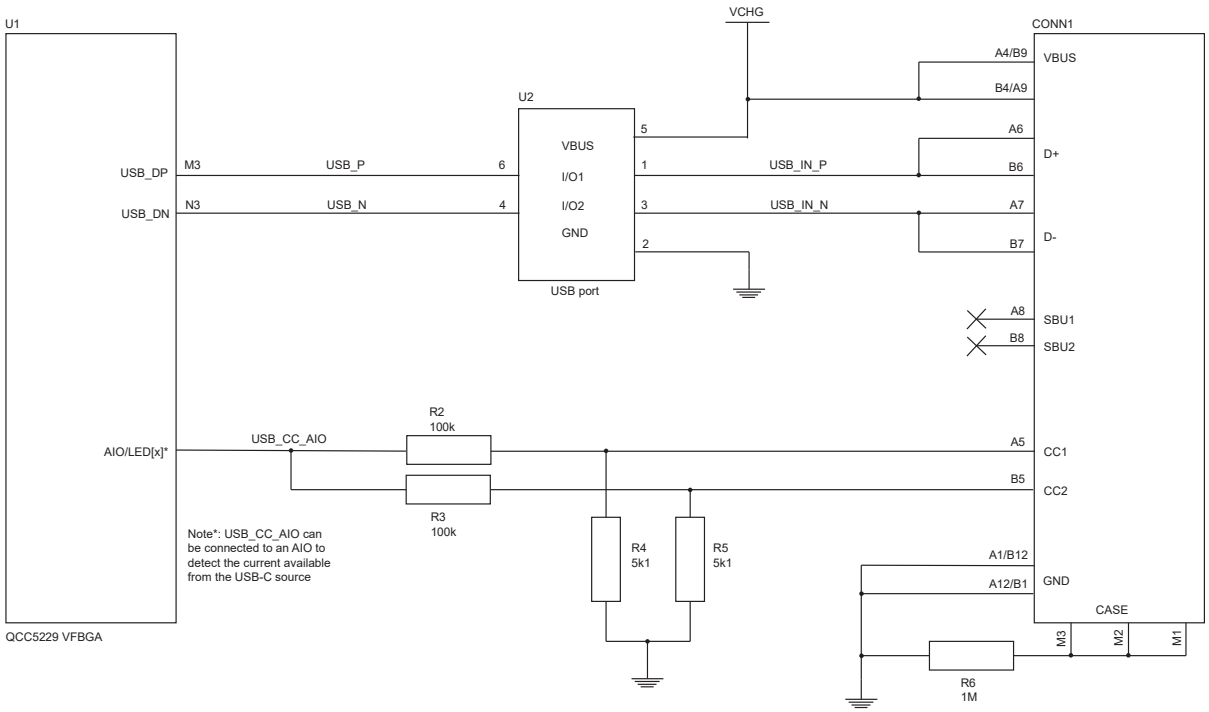

Figure 11-1 QCC5229 VFBGA USB circuit diagram

Schematic

The VCHG input of the QCC5229 VFBGA is tolerant of a constant 6.5 V and transients up to 7.0 V. If additional over voltage protection is required, use external clamping protection devices.

For system-level ESD protection on USB pins, see System level ESD protection.

11.2 USB connections

All USB standards and connectors are specified to ensure that the ground connection is made first and breaks last, ensuring a correct and stable ground reference for charger detection and USB communications.

Design any nonstandard, for example, pogo pins or snap contact connectors, in the same way to ensure a good ground connection is maintained reliably. This design includes positioning a ground connection at either end to ensure that a slightly lifted connection still maintains a ground connection.

This design is important if the other end of the USB cable is made available as a standard type A or C connector, which could be used with alternative chargers by the end user. There is a risk that a USB connection with intermittent ground connection or missing ground connection could be misinterpreted by some alternative chargers as a command to increase their VBUS voltage to higher voltages, leading to damage of the downstream device.

The QCC5229 VFBGA can connect to the central data pins, and the four VBUS pins of the USB-C® connector. The connector ensures correct connection in either orientation. Leave the unused connector pins unconnected.

For simple charger detection of 1.5 A and 3.0 A capable chargers, the two USB CC lines can be individually terminated with the required 5.1 k resistor. Then use a single LED/AIO input by high impedance combination to sense the CC line voltage thresholds.

Charging only USB port

Connect VCHG and VBUS as in Figure 11-1. Leave the USB_DP and USB_DN pins unconnected. This connection allows USB charger detection to complete and enter the **Data lines floating** charger type.

No USB connection

Leave USB_DP and USB_DN pins unconnected.

11.3 Layout notes

Keep the USB data line tracks between the connector and the QCC5229 VFBGA short, with minimum layer changes, and a continuous ground path beneath the data tracks.

Over longer distances, route the USB data lines as a 90 Ω differential pair. These data lines should have a single-ended impedance to ground of around 45 Ω and a track length matched to avoid skew.

Route USB tracks away from the RF and crystal sections of the system to avoid interference.

Avoid the stubs on the data lines and keep to a minimum where unavoidable, such as USB-C connectors.

12 System level ESD protection

Sufficient system-level ESD protection is critical to develop reliable products.

Schematic

The required protection devices and their location depend on both the electrical and mechanical design of a product. External devices such as TVS diodes are required on terminals that are exposed to the end user as well as components mounted behind apertures in the product enclosure. If TVS diodes are used, they should be placed between signal traces and grounded to limit ESD induced voltages/currents and to protect the QCC5229 VFBGA. The TVS diodes should be appropriately sized for the voltage level of the signal and the maximum rating of the pin.

The following devices/interfaces require protection devices:

- USB
- Speaker driver
- Microphone
- Line input
- Push button

Figure 12-1 through Figure 12-5 show examples of adding protection devices to the USB, speaker, microphone, line input, and push button.

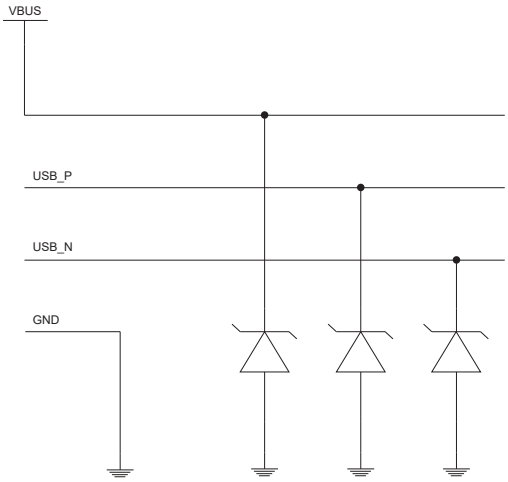

Figure 12-1 ESD protection for USB

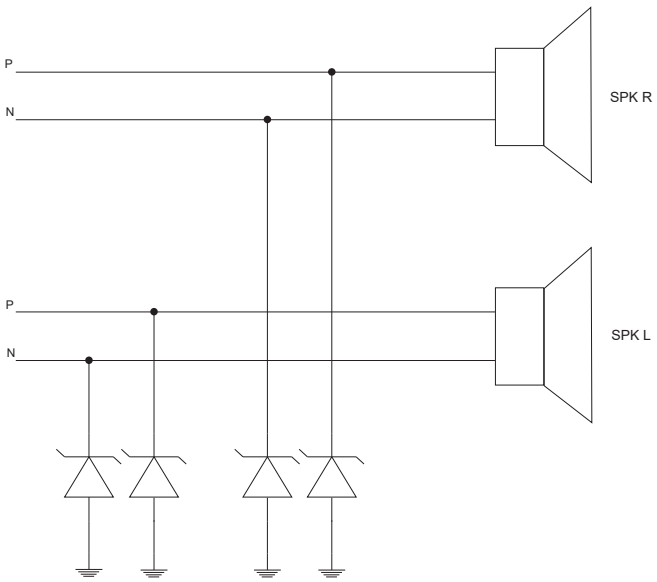

Figure 12-2 ESD protection for speaker

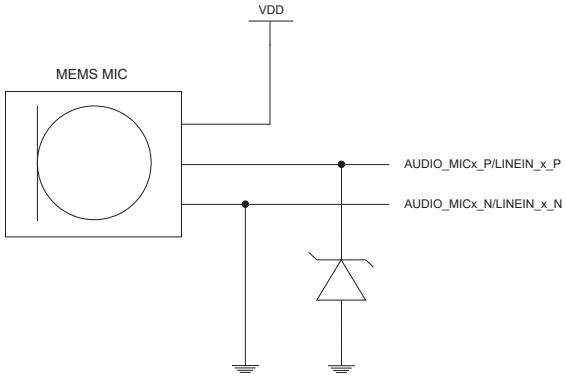

Figure 12-3 ESD protection for microphone

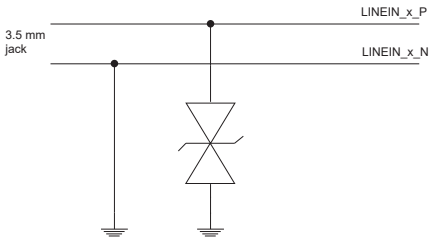

Figure 12-4 ESD protection for line input

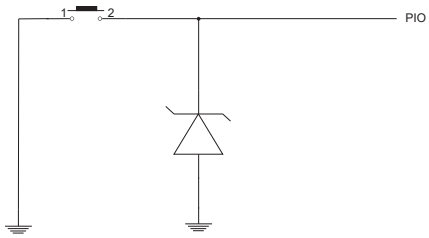

Figure 12-5 ESD protection for push button

When not activated by an ESD event, TVS diodes act as a capacitor. When selecting parts, ensure to protect high-speed or switching interfaces such as USB, digital microphone interfaces, and Class-D headphone outputs. Capacitance should be minimized as it may impact signal integrity and cause additional power consumption.

The QCC5229 VFBGA incorporates device level ESD protection into all terminals, which is intended to protect the device through the manufacturing and PCB assembly process. For more information, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

A QCC5229 VFBGA example application schematic and BOM

QCC5229 VFBGA example application schematic

Figure A-1 through Figure A-4 show the example application schematic for the QCC5229 VFBGA.

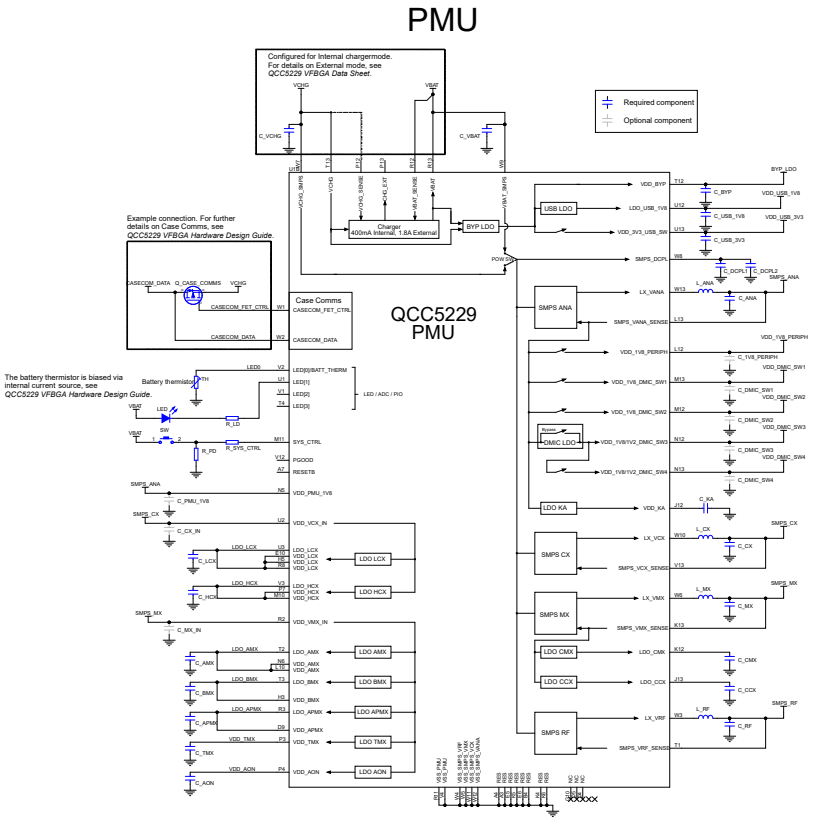

Figure A-1 QCC5229 VFBGA example application schematic: PMU

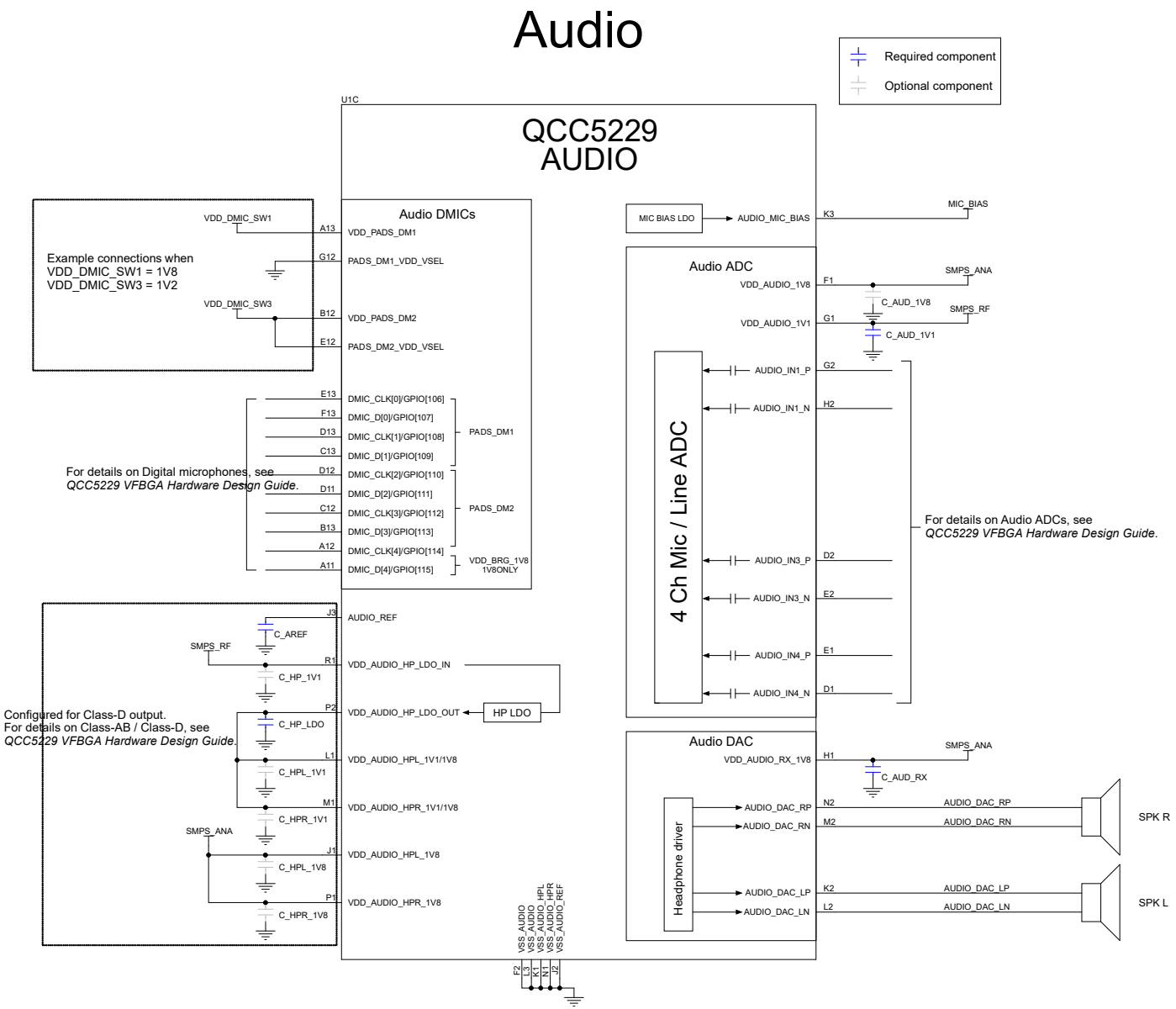

Figure A-2 QCC5229 VFBGA example application schematic: Analog audio, DMIC, and LEDs

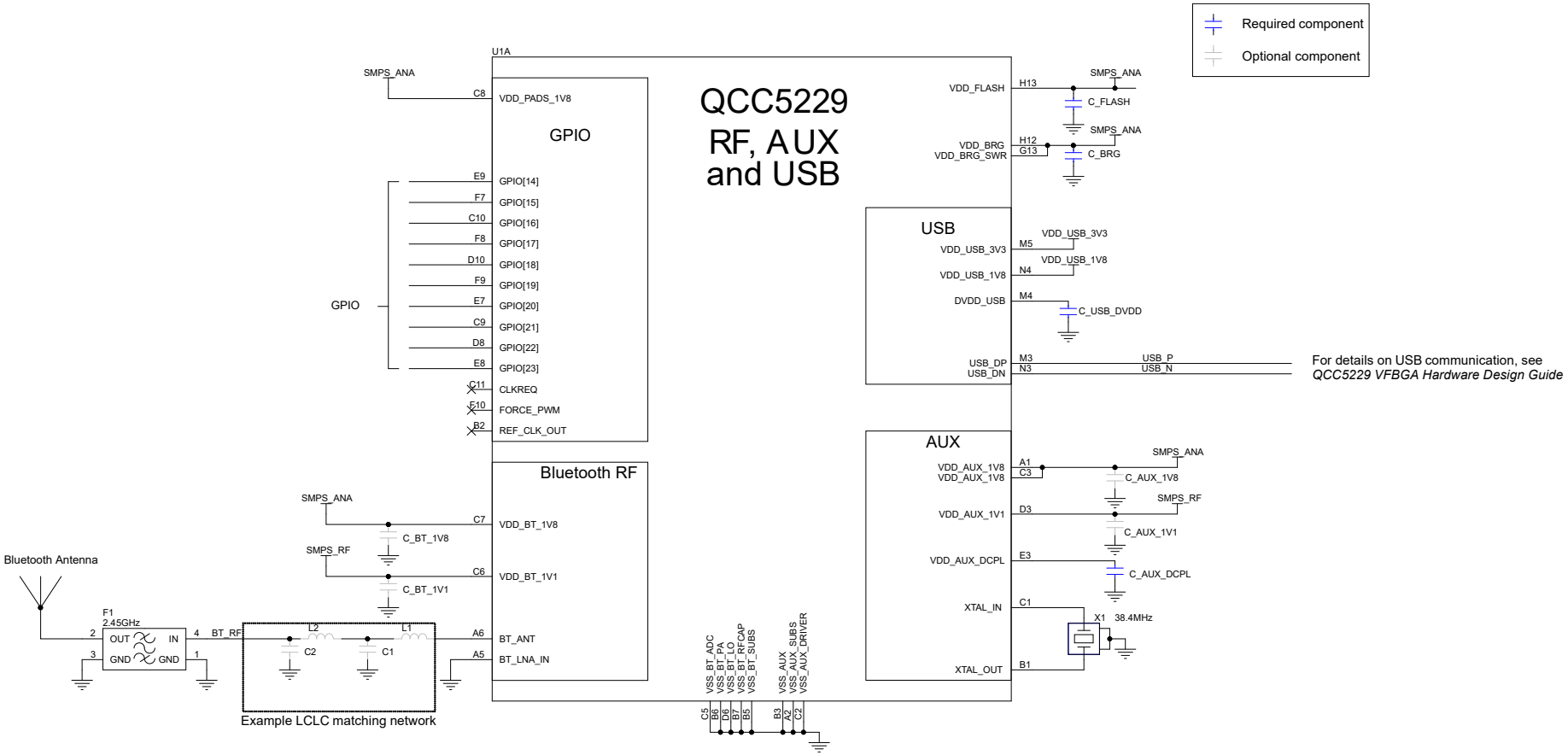

Figure A-3 QCC5229 VFBGA example application schematic: Bluetooth RF, AUX, and USB

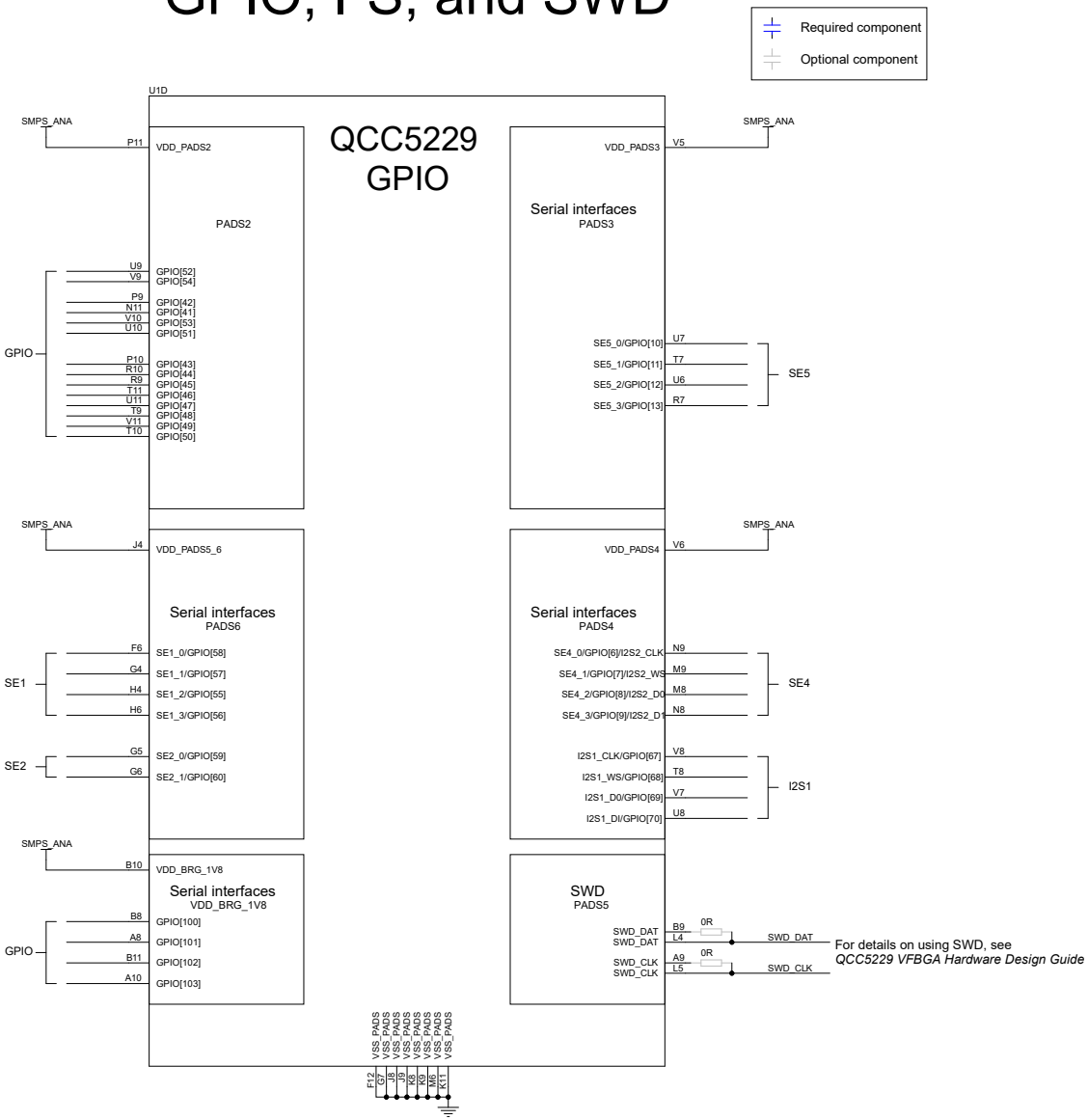

Figure A-4 QCC5229 VFBGA example application schematic: GPIO, I²S, and SWD

QCC5229 VFBGA bill of materials

Table A-1 lists the bill of materials (BOM) of the system components for the QCC5229 VFBGA example application schematic shown in this document.

For more information about the QCC5229 VFBGA, see *QCC5229 VFBGA Data Sheet* (80-75559-1).

NOTE Table A-1 is an example BOM of the reference design, the component values and ratings should be used as reference only.

Table A-1 QCC5229 VFBGA bill of materials

Item no.	Qty req.	Circuit ref.	Example value	Example tolerance	Example package (metric)[a]	Example manufacturer	Example manufacturer's part no.
1	1	U1	QCC5229 V FBGA	-	-	Qualcomm	-
2	1	F1	2.45 GHz	-	FILTER MURATA LFB182G45SG9B740	Murata	LFB182G45CE6D131
3	1	X1	38.4 MHz	-	CRYSTAL SIWARD 1612	SIWARD INTERNATIONAL INC	XTL901-Q23-065
4	1	SW	-	-	SWITCH TACTILE SMT ITT KSR	ITT	KSR231G LFS
5	1	Q_CASE_COMMS	-	-	DFN603-3	NEXPERIA	PMX400UPZ
6	2	C_AMX, C_HCX	2.2 µF	10%	0201	Murata	GRM033R61A225KE47D
7	7	C_ANA, C_CX, C_DCPL2, C_MX, C_RF, C_VBAT, C_VCHG	10 µF	20%	0402	Murata	GRM155R61A106ME11D
8	13	C_AON, C_APMX, C_AUD_1V1, C_AUD_RX, C_BMX, C_CCX, C_CMX, C_HP_LDO, C_KA, C_LCX, C_TMX, C_USB_1V8, C_USB_3V3	1 µF	20%	0201	Murata	GRM033R61A105ME15D
9	2	C_BYP, C_AREF	2.2 µF	10%	0402	Murata	GRM155R61C225KE11J
10	3	C_AUX_DCPL, C_DCPL1, C_USB_DVDD	10 nF	10%	0201	AVX	0201YC103KAT2A
11	2	C_BRG, C_FLASH	100 nF	10%	0201	Murata	GRM033Z71A104KE14D
12	4	L_ANA, L_CX, L_MX, L_RF	2.2 µH	20%	0603	Taiyo	LSCNB1608HKT2R2MD
13	1	LED	Red	-	0402	Kingbright	KPHHS-1005SURCK
14	1	R_LD	470 Ω	1%	0402	Panasonic	ERJ2RKF4700X

Table A-1 QCC5229 VFBGA bill of materials (cont.)

Item no.	Qty req.	Circuit ref.	Example value	Example tolerance	Example package (metric)[a]	Example manufacturer	Example manufacturer's part no.
15	1	R_PD	10 kΩ	1%	0402	VISHAY	CRCW040210K0FKED
16	1	R_SYS_CTRL	100 kΩ	5%	0402	KOA	RK73B1ETTP104J
17	1	TH	10 k	3%	0402	Murata	NCP15XH103J03RG

[a] 1005 (metric) / 0402 (imperial), 0603 (metric) / 0201 (imperial), 1608 (metric) / 0603 (imperial).

B Recommended crystal specification

This section describes the key specification requirements for crystals to be used with the QCC5229 VFBGA.

B.1 Electrical requirements

Table B-1 lists performance to be met over operating temperature range unless otherwise stated.

Table B-1 Electrical requirements

Parameter	Min	Typ	Max	Unit	Notes
Operating frequency	-	38.4	-	MHz	-
Initial frequency tolerance	-20	-	20	ppm	At 25°C ± 3°C
Frequency drift after reflow	-20	-	20	ppm	After 2 reflows
Tolerance over temperature	-20	-	20	ppm	-30°C to 85°C
Aging	-20	-	20	ppm	5 years
Frequency perturbations	-20	-	20	ppm	
Operating temperature	-40	-	105	C	
Storage temperature	-40	-	105	C	
ESR	-	-	60	Ω	
Spurious mode series resistance	1100	-	-	Ω	
Motional inductance	-	-	20	mH	
Shunt capacitance	-	-	1.0	pF	
Load capacitance	6			pF	
Drive level	0.01	100	200	µW	
Insulation resistance	500	-	-	MΩ (100 V)	

B.2 Recommended crystals

The parts in Table B-2 meet the specification detailed in this document and are tested by QTIL. Ensure that the oscillator has sufficient margin in the design with any crystal resonator you select.

Table B-2 QCC5229 VFBGA recommended crystals

Frequency	Temperature range	Package	Manufacturer	Part number
38.4 MHz	-40°C/ 105°C	1612	Siward	XTL901-Q23-065

C Recommended RF filter specification

This section describes the key specification requirements for radio frequency (RF) band pass filters for QCC5229 VFBGA applications.

NOTE Correct PCB layout is critical to achieve the data sheet performance of LTCC band pass filters.

C.1 Electrical requirements

Table C-1 lists performance to be met over operating temperature range unless otherwise stated.

Table C-1 Electrical requirements

Parameter	Frequency (MHz)	Min	Typ	Unit
Characteristic impedance		-	50	Ω
Attenuation	4800 to 5000 (second harmonic)	12.3	-	dB
	7200 to 7500 (third harmonic)	31		
	1200 to 1250	12		
	1800 to 1875	5		
	3000 to 3125	5		
	3600 to 3750	5		
	5400 to 5625	14		
	9600 to 10000	20		
	12000 to 12500	13		

NOTE Attenuation requirements could change based on antenna frequency response. Values provided in the table are assuming 10 dB attenuation at the second harmonic and 0 dB at the third harmonic.

Document references

Document	Reference, date
QCC5229 VFBGA Data sheet	80-75559-1
Qualcomm Charger Case Communication Specification	80-21985-1

Glossary

Term	Definition
AIO	Analog input/output
Bluetooth	Set of technologies providing audio and data transfer over short-range radio connections
BOM	Bill of materials
BTL	Bridge-tied load
DCM	Discontinuous conduction mode
EMI	Electromagnetic interference
GND	Ground
IC	Integrated circuit
I²C	Inter-integrated circuit interface
I²S	Inter-integrated circuit sound
Kbps	Kilobits per second
LDO	Low (voltage) drop-out
LED	Light-emitting diode
LTCC	Low temperature co-fired ceramic
Mbps	Megabits per second
MEMS	Micro electro mechanical system
PCB	Printed circuit board
PCM	Pulse code modulation
PFM	Pulse frequency modulation
PIO	Programmable input/output, also known as general-purpose I/O
ppm	parts per million
PSU	Power supply unit
PWM	Pulse width modulation
QTIL	Qualcomm Technologies International, Ltd.
RF	Radio frequency

Term	Definition
SAW	Surface acoustic wave
SMPS	Switch-mode power supply
UART	Universal asynchronous receiver transmitter
ULP	Ultra low power
USB	Universal serial bus

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